U S E R ' S   M A N U A L

GPS
TIMING
M-MODULE

MODEL
M213

Document Part No: 11029064A

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NOTE

The contents of any amendment may affect operation, maintenance, or calibration of the equipment.

INTRODUCTION

This manual describes the operation and use of the C&H Model M213 GPS Timing M-Module (Part Number 11029060). This mezzanine module is designed to interface within any M/MA-Module carrier adhering to the ANSI/VITA 12-1996 M-Module specification. These carriers are available in many formats such as VME, VXI, PXI, cPCI, and the PC.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction using the higher level interface provided by the driver.

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1.0 GENERAL DESCRIPTION

The M213 provides GPS timing in a single-wide M-Module format adhering to the ANSI/VITA 12-1996 specification for M-Modules. The M213 may be installed on any carrier board supporting the M-Module specification. Carriers are available that allow the M213 to be used in VXI, VME, PCI, cPCI and many other system architectures.

1.1 PURPOSE OF EQUIPMENT

The M213 can be used in a wide variety of applications where a precision timing control is required.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Module Key Features

- ANSI Standard M-Module (single-wide)
- Motorola Oncore M12+ GPS Timing Receiver
- M-module interface allows complete communication with M12+
- Active monitoring of PPS output indicates when a valid 1PPS output signal is available
- PPS output control (always off, always on, or on when certain conditions are met)
- Antenna bias power is switch selectable for +3V or +5V operation.
- External power pass-through for integration with other M-modules

1.2.2 Oncore M12+ Specific Features:

- 12-channel parallel receiver design tracks up to 12 satellites simultaneously
- Code plus carrier tracking (carrier-aided tracking)
- Position filtering
- Antenna current sense circuitry
- 3-dimensional positioning within 25 meters, SEP (with Selective Availability [SA] disabled)
- Extensive control and status
  - Satellite tracking
  - PPS output control
  - Latitude and longitude
  - Height
  - Time
- Selectable 1 or 100PPS output
- Time-Receiver Autonomous Integrity Monitoring (TRAIM) algorithm for checking timing solution integrity
- Automatic site survey

1.2.3 Specifications

MAXIMUM RATINGS

Parameter	Condition	Rating	Units
Operating Temperature		0 to +50	°C
Non-Operating Temperature		-40 to +70	°C
Humidity	non-condensing	5 to 95	%
Power Consumption	+5V +12V or EXTPWR (at +12V) -12V	0 130 0	mA mA mA
Input Voltage	EXTPWR	40	V
Supply Current	EXTPWR Pass-Through	2.0	A

AC CHARACTERISTICS

Parameter	Conditions	Specification	Units
GPS Timing General Characteristics			
- Receiver		12	channels
- Tracking capability	simultaneous vehicles	12	satellites
- Operating Frequency	L1	1575.42	MHz
GPS Timing Performance Characteristics			
- Acquisition Time, Time to First Fix (TTFF)	Hot (almanac, position, time, ephemeris) Warm (almanac, position, time) Cold (no stored information) Internal Reacquisition after blockage	<25 <50 <200 <1	sec. sec. sec. sec.
- Positioning accuracy	selective availability disabled	<25	meters SEP
- Timing accuracy [1]	using clock granularity message 1σ average 6σ average without clock granularity message 1σ average 6σ average	 <2 <6 <10 <20	 ns ns ns ns
- Antenna requirements	Active antenna module with external gain Required gain [2] Bias Power Current draw	 18-36 3 or 5 80	 dBm V mA max.
PPS Output Electrical Characteristics (Front panel and internal connector)			
- Output Level	High (V_{OH}) into 50Ω load Low (V_{OL}) into 50Ω load	2.0 0.4	V min. V max.
- Output Impedance		50 ±3	Ω
- Output Source/Sink Current		±50	mA
- Propagation delay	from M12+ output	3.5 min., 9.0 max.	ns
- Skew	front panel output to internal connector output (common-edge variation)	300	ps max.
- Rise/Fall Time	from 0.8V to 2.0V / 2.0V to 0.8V	1.5	ns max.
PPSACT Output Electrical Characteristics (Front panel)			
- Output Level	High (V_{OH}) into high impedance load Low (V_{OL}) into high impedance load	2.4 0.5	V min. V max.
- Output Impedance		3 to 7	Ω typ
- Output Source/Sink Current		±24	mA
External Power Supply			
- Input Voltage		+10 to +30	Vdc

Notes:
1. 1PPS or 100PPS with position-hold active
2. As measured at the M12+ RF connector

1.2.4 Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for single-wide M-Module modules. The nominal dimensions are 5.687" (144.5 mm) long × 2.082" (106.2 mm) wide.

1.2.5 Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for single-wide M-Modules and the MA-Module trigger signal extension. The module also supports the optional IDENT and VXI-IDENT functions.

Module Type:	M-Module
Addressing:	A08
Data:	D8
Interrupts:	INTA & INTC
DMA:	not supported
Triggers:	not supported
Identification:	IDENT and VXI-IDENT
Manufacturer ID:	$0FC1_{16}$
Model Number:	$00D5_{16}$ (213 dec.)
VXI Model Code:	$0FDD_{16}$ (M213)

1.2.6 Applicable Documents

ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, www.vita.com

User's Guide, Motorola M12+ GPS Positioning And Timing Receivers, Synergy Systems, LLC, P/N STRMM12+ Rev. A, 24 Nov 03, P.O. Box 262250, San Diego, CA 92196, www.synergy-gps.com

User's Guide, GPS Oncore Revision 5.0, Motorola GPS Products, 08/30/02, www.motorola.com

2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

Verify that there has been no damage to the shipping container. If damage exists then the container should be retained, as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The M213 contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION OF M/MA MODULES

All M-Modules must be installed into the carrier before the carrier is installed into the host system. To install a module, firmly press the connector on the M/MA-Module together with the connector on the carrier as shown in Figure 1. Secure the module through the holes in the bottom shield using the original screws.

> **CAUTION: M/MA-Module connectors are NOT keyed. Use extra caution to avoid misalignment. Applying power to a misaligned module can damage the M/MA-Module and carrier.**

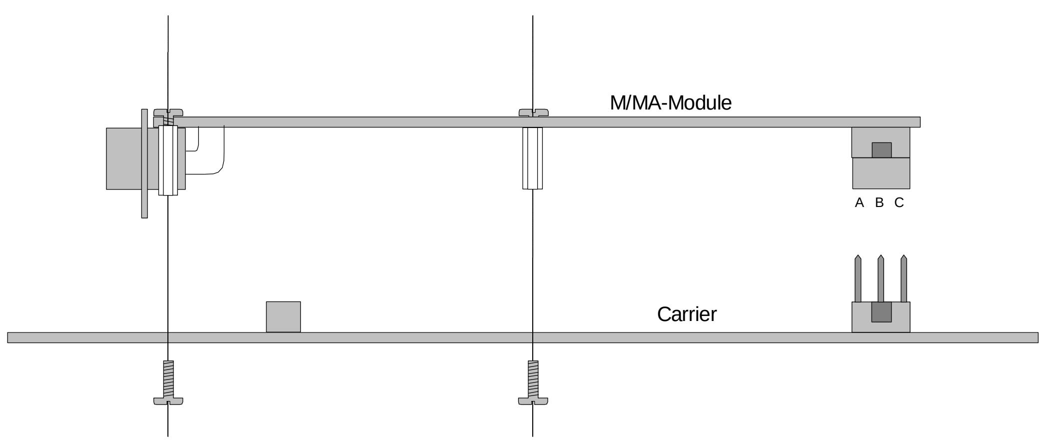

Figure 1. M-Module Installation

2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti-static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum. The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

3.0 FUNCTIONAL DESCRIPTION

3.1 OVERVIEW

The M213 utilizes control logic to interface the M-Module bus to a Motorola Oncore M12+ Timing Receiver. The M12+ is controlled internally through a serial interface. See applicable documents in Section 1.2.6 for details on the M12+. A simplified block diagram is shown in Figure 2.

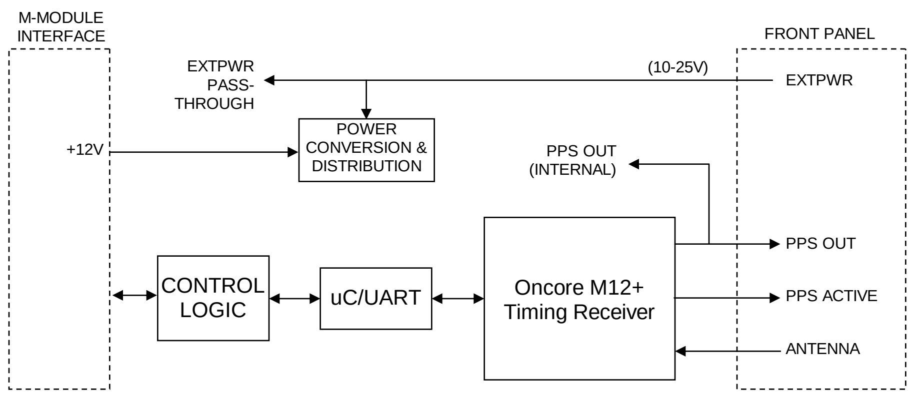

Figure 2. Functional Block Diagram

3.1.1 M-Module Interface

The M-Module Interface allows communication between the M213 and the carrier module. The interface is an asynchronous 16-bit data bus with interrupt capabilities. The interface adheres to the ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification for M modules.

3.1.2 Control Logic

The control logic provides the electrical interface between the M-module bus and the module. The control registers are contained within this logic. The control registers are described in Section 3.4.1. The control logic also monitors the PPS output and indicates when a valid 1PPS or 100PPS output signal is available (PPSACT). Status is visually indicated on the front panel and is available through an M-module register. An interrupt can also be generated on any change of status.

3.1.3 Microcontroller/UART

The microcontroller/UART provides the communication to and from the M12+ Timing module. An internal FIFO facilitates the software communication.

3.1.4 Oncore M12+ Timing Receiver

The M12+ is GPS Timing Receiver module from Motorola. The M12+ internally provides extensive control and status of the GPS timing receiver, including antenna connection feedback, satellite tracking status, output quality indication, 1PPS output control, and a host of other position, almanac, and timing status and control functions. Detail information on this module can be found in the applicable documents shown in Section 1.2.6.

3.1.5 Power Conversion and Distribution

The main power for the module is obtained from either the M-module interface (+12V) or from an external supply through the front panel connector. Power is converted to appropriate levels and distributed to the individual components on the M213. The module uses the +12V supply from the M-module interface, unless an external supply is provided that is greater than +12V. To maintain GPS tracking, when the M-module interface is not powered, an external power supply must be provided.

To support integration with other M-modules, an external power pass-through connector is provided that simply passes the external supply voltage through, if it exists.

3.2 PHYSICAL LAYOUT

The physical layout of the module is shown in Figure 3. Notched in the PCB are provided for cabling to the external power pass-through and the internal PPS output when the module is installed adjacent to other M-modules. A switch is provided to set the antenna bias voltage to either +3V or +5V.

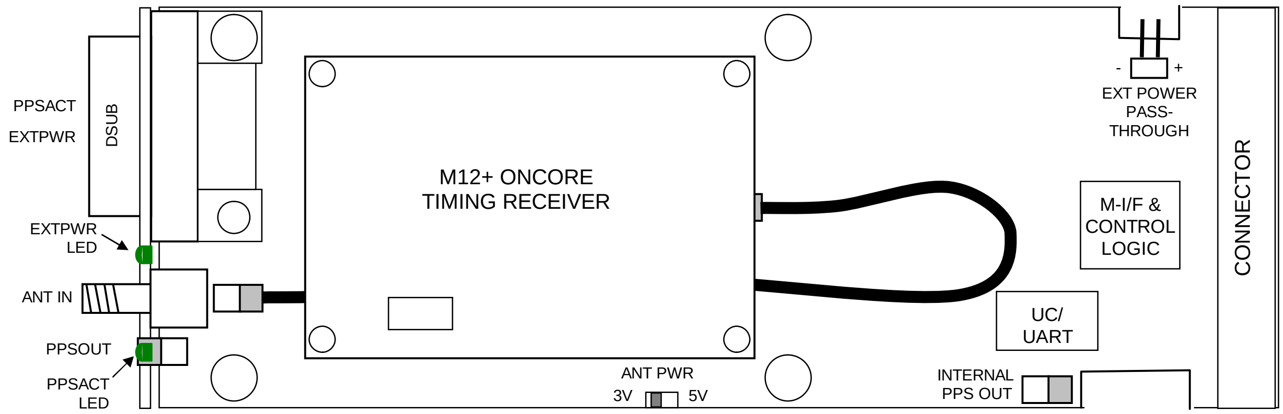

Figure 3. M213 Physical Layout

3.3 INPUT/OUTPUT SIGNALS

The front panel input/output signals are as shown in Figure 4 and are briefly described below.

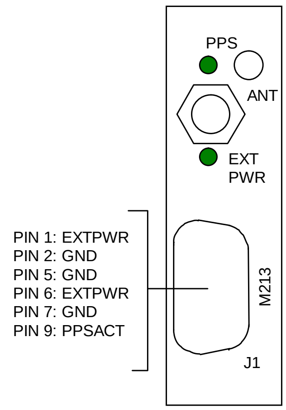

Figure 4. Front Panel

<u>PPS</u> This MMCX connector provides the PPS output signal from the timing receiver. The signal is buffered through a 50Ω clock distribution driver. Under software control of the timing receiver, the output may be always ON, always OFF, or only ON if certain conditions are met. The LED indicates the ON/OFF status of the signal. The LED is visual indicator of the PPSACT signal (see below). *(5V CMOS logic levels, 50Ω output impedance)*

<u>ANT</u> This SMA jack is for the antenna input. The bias voltage may be selected for 3V or 5V operation. *(see Section 1.2.3 for antenna requirements)*

<u>EXTPWR</u> These two DSUB pins provide power to the M213 and to the external power pass-through connector. Module power can be provided through these front connectors or through the M-module +12V interface. The EXTPWR LED illuminates when external power above 8 to 10 volts is applied to the DSUB connector pins. *(+10 to +30Vdc)*

<u>PPSACT</u> This DSUB pin indicates the status of the PPS output signal. The signal is high when the PPS signal is active. The PPS output from the GPS timing receiver is continuously monitored by the control logic. If the PPS output does not pulse within 1.3 seconds, the PPSACT signal will indicate inactive. *(active high, TTL output, low output impedance)*

<u>GND</u> These DSUB pins are the return paths for the EXTPWR and the PPSACT signals. The pins are connected to the logic ground on the module.

3.4 IDENTIFICATION AND CONFIGURATION REGISTERS

3.4.1 I/O Registers

There are a variety of registers used to configure and control the M213 module. These registers are located in the IOSpace. The address map of the registers is shown in Table I. Details of the registers are provided in Figure 5.

Table I. I/O Address Map/Command Summary

M213 IO REG. (HEX)	REGISTER DESCRIPTION
00	Control/Status
02	Interrupt Control
04	UART Data Registers

M213
Reg. 00

Control/Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								-	-	-	-	-	-	-	-
Read	Not Used								-	-	-	-	-	-	PPS	-

PPS ⇨ PPS Active (0 = PPS output is not active, 1 = PPS output is active)

M213
Reg. 02

Interrupt Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								IT	-	-	-	MIEN	-	PIEN	UIEN
Read	Not Used								IT	-	PPSI	URTI	MIEN	-	PIEN	UIEN

IT ⇨ Interrupt Type (0 = Type A, software-end-of-interrupt (default), 1 = Type C, hardware-end-of-interrupt)
PPSI ⇨ PPS Interrupt Pending (1 = a PPS interrupt is pending (write a 1 to this bit to clear))
URTI ⇨ UART Interrupt Pending (1 = a UART interrupt is pending (write a 1 to this bit to clear))
MIEN ⇨ Master Interrupt Enable (0 = disabled (default), 1 = enable)
PIEN ⇨ PPS Interrupt Enable (0 = disabled (default), 1 = enabled)
UIEN ⇨ UART Interrupt Enable (0 = disabled (default), 1 = enabled)

Note: When using Type C interrupts (IT = 1), the interrupt pending bits 7-0 are presented as the interrupt vector during the interrupt acknowledge cycle. The MIEN bit is also cleared and must be re-enabled during the interrupt service routine. A PPSI interrupt occurs, if enabled, on any change of status of the PPS signal. A URTI interrupt only occurs when data is available.

M213
Reg. 04

UART Data Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								Data							
Read	Not Used								Data							

Note: A write to Data transmits the byte to the M12+ timing receiver module. A read of Data receives one byte of data from the M12+ receive FIFO. A “Special Character, 0xFF” indicates that the FIFO is empty. URTI = 0 also indicates the FIFO is empty.

Figure 5. M213 I/O Registers

3.4.2 M-Module Identification PROM

The M213 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in a sixteen-word deep (32 byte) serial EEPROM. Access is accomplished with read/write operations on the last address in IOSpace (hex FE) and the data is read one bit at a time. Instructions for reading the IDENT PROM are given in section 4.3.

The module also supports the VXI-IDENT function. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the EEPROM to at least 64 words (128 bytes) and includes VXI compatible ID and Device Type Registers. Details are shown in Table II.

Table II. M-Module EEPROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	00D5 (213 dec.)
2	Revision Number[1]	0001
3	Module Characteristics[2]	1068
4-7	Reserved	0000
8-15	M-Module Specific	0000
16	VXI Sync Code	ACBA
17	VXI ID	0FC1 (C&H)
18	VXI Device Type[3]	FFDD (M213)
19-31	Reserved	0000
32-63	M-Module Specific	0000

Notes:

1) The Revision Number is the functional revision level of the module. It does not necessarily correspond to the hardware assembly level.
2) The Module Characteristics bit definitions are:

Bit(s)	Description
15	0 = no burst access
14/13	unused
12	1 = module needs ±12V
11	0 = module does not need +5V
10	0 = trigger outputs not supported
9	0 = trigger inputs not supported
8/7	00 = no DMA requestor
6/5	11 = interrupt type C
4/3	01 = 16-bit data
2/1	00 = 8-bit address bus
0	0 = no memory access

3) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	FDD_{16} = C&H specified VXI model code for M213

4.0 OPERATION

The M213 is a register-based instrument that is controlled through a series of I/O registers described in Section 3.4.1. The exact method of accessing and addressing the I/O registers is dependent on the M-Module carrier used to interface the module to your data acquisition or test system. Refer to the carrier's documentation for information on the address mapping of an M-Module's I/O registers and to your system software documentation for details on data access. A high-level driver may also be available for control.

4.1 TIMING RECEIVER COMMUNICATION

The UART Data Register is used to communicate with the M12+ Timing Receiver module. Data written to the register is serially transmitted to the M12+. Serial data received from the M12+ is converted into 8-bit data bytes and stored in a FIFO to be read by the user. The FIFO can store approximately 512 bytes. See Chapter 5 , "I/O COMMANDS" in the Motorola M12+ GPS Positioning And Timing Receivers User's Guide" for command details.

4.2 INTERRUPTS

The M213 supports Type A and Type C interrupts as specified in the M-module specification. A Type A interrupt releases the interrupt request only after the pending interrupt is cleared by software (software-end-of-interrupt (i.e., RORA)). A Type C interrupt releases the interrupt request during the interrupt acknowledge cycle (hardware-end-of-interrupt with vector (i.e., ROAK)) Type C interrupts provide an interrupt vector during an interrupt acknowledge cycle. Use the IT bit in the Interrupt Control Register to configure the desired type of interrupt.

> NOTE: For any interrupt to occur, the MIEN bit in the Interrupt Control Register must be set to a one.

For an interrupt to occur, the desired interrupt source must be enabled (PIEN or UIEN) and the master interrupt enable (MIEN) must be enabled in the Interrupt Control Register. For Type C interrupts, the interrupt vector is equal to the lower byte of the interrupt control register.

> NOTE: When using Type C interrupts, the MIEN bit is cleared during the interrupt acknowledge cycle. It must be re-enabled to receive another interrupt.

4.3 ID PROM

Refer to 3.4.2 for a description of the ID PROM's function and contents. The ID PROM is a serial device and accessing it involves writing and reading a register in a sequential manner to acquire data. Figure 6 provides a general description of the code sequence necessary to read the information from the PROM. The PROM is a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet.

```
/*--------------------------------------------------------------------*/
int read_idword (unsigned short id_addr, unsigned short *value){
  addr = 0xFE;                          /* M/MA address for IDPROM */
  id_addr = 0x80 | id_addr;             /* 80 is the read opcode for the PROM */
  write_eebyte (addr, id_addr);
  read_eebyte (addr,&rdval);            /* returns first byte of IDPROM */
  tmpval = rdval << 8;                  /* upper byte of sync code word */
  read_eebyte (addr,&rdval);            /* returns first byte of IDPROM */
  tmpval = tmpval | rdval;              /* combine bytes of sync code   */
  *value = tmpval;
  write_word(addr, 0x0000);             /* lower cs */
  return;
}
/*--------------------------------------------------------------------*/
int write_eebyte (unsigned long addr, unsigned short value){
  write_word(addr, 0x0000);             /* insure cs is initially low */
  write_word(addr, 0x0004);             /* initialize */
  write_eebit(addr, 0x0001);            /* start bit */
  temp = value;
  for (i=0;i<=7;i++){
    write_eebit(addr, ((temp & 0x80)>>7));
    temp = (temp << 1);
  }
return;
}
/*----------------------------------------------------------------------*/
int write_eebit (unsigned long addr, unsigned short value){
  temp = (0x0004 | (value & 0x0001));   /*  set data bit before clock */
  write_word(addr, temp);
  Delay(.000005);
  temp = (0x0006 | (value & 0x0001));   /*  set data bit & clock */
  write_word(addr, temp);
  Delay(.000005);
  return;
}
/*--------------------------------------------------------------------*/
int read_eebyte (unsigned short addr, unsigned short *value){
  for (i=7;i>=0;i=i-1){
    read_eebit (addr, &rdval);
    temp = temp | ((rdval&0x01) << i);
  }
  *value = temp;
  return;
}
/*-----------------------------------------------------------------------*/
int read_eebit (unsigned short addr, unsigned short *value){
  write_word(addr, 0x4);                /* lower clock bit */
  Delay(.000005);
  write_word(addr, 0x6);                /* raise clock bit */
  Delay(.000005);
  read_word (addr, value);
  return;
}
/*-----------------------------------------------------------------------*/
```

NOTE: 1. write_word and read_word are low level memory access routines.
*2. **NOT** actual code and should be treated as a modeling tool only.*

Figure 6. ID PROM Access Routine

APPENDIX A: CONNECTORS

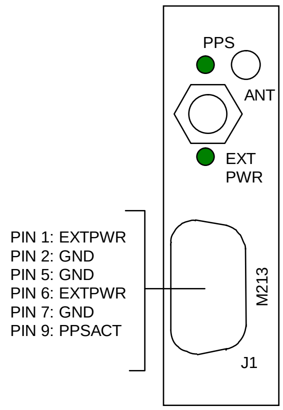

Figure A-1. Front Panel I/O Signals

Pin	Row A	Row B	Row C
1	/CS	GND	(/AS)
2	A01	+5V	(D16)
3	A02	+12V	(D17)
4	A03	-12V	(D18)
5	A04	GND	(D19)
6	A05	(/DREQ)	(D20)
7	A06	(/DACK)	(D21)
8	A07	GND	(D22)
9	D08	D00/(A08)	TRIGA
10	D09	D01/(A09)	TRIGB
11	D10	D02/(A10)	(D23)
12	D11	D03/(A11)	(D24)
13	D12	D04/(A12)	(D25)
A14	D13	D05/(A13)	(D26)
15	D14	D06/(A14)	(D27)
16	D15	D07/(A15)	(D28)
17	/DS1	/DS0	(D29)
18	DTACK	/WRITE	(D30)
19	/IACK	/IRQ	(D31)
20	/RESET	SYSCLK	(/DS2)

Note: Signals in parentheses ( ) are not used on this module.

Figure A-2. M/MA Interface Connector Configuration

N O T E S:

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F. R. Harrison
President and CEO

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