

U S E R ' S M A N U A L

VME  
PROTOTYPING  
MODULE

MODEL  
VM100

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## **INTRODUCTION**

This manual describes the operation and maintenance of the C&H Model VM100 VME Prototyping Module (Part No. 11026010). This module is one of a number of test and data acquisition/control modules in the VME and VXI format provided by C&H.

Contained within this manual is information on the physical and electrical specifications, installation and startup procedures, operating procedures, functional analysis, and figures and diagrams required to adequately support this product.



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## 1.0 GENERAL DESCRIPTION

The VME Prototyping Module is a VMEbus compatible B size module with over 34 square inches of user space.

### 1.1 PURPOSE OF EQUIPMENT

This module is well suited for applications in prototyping VMEbus designs, proof of concept testing, and design verification. The VME Prototyping Module provides all necessary VMEbus register interface functions, and the user interconnect terminals to reduce design time and effort.

### 1.2 SPECIFICATIONS

#### 1.2.1 Key Features

- Over 34 square inches of usable layout space
- Signal names silkscreened on both the component and solder sides
- Prototyping holes on a 0.1" by 0.1" grid
- VCC and GND strips along top and bottom edges
- User interface signals provided:
  - D00 to D015 - Buffered VMEbus Bi-directional data
  - WR0 to WR7 - Write Gates
  - READ0-1/ to READ6-7/ - Read Gates
  - LDTACK - Local Data Acknowledge
  - RST/ - Reset
  - A01 to A03 - Buffered VMEbus addresses
  - SEL/ - A23 to A08 address decode
  - WR/ - Data Bus direction control signal
  - DS0/, DS1/ - Buffered Data Strokes
  - UUP=Q/ - Address Bits A31 to A24 decode input

#### 1.2.2 Electrical

The VME interface circuitry provided on the module requires +4.5V to +5.5V at 0.5 amps for proper operation. The actual power requirements will depend on the user's circuitry.

#### 1.2.3 Mechanical

The mechanical dimensions of the module is in conformance with the VMEbus specification (Rev. C.1) for single slot size 'B' modules. The nominal dimensions are 233.35mm (9.187 in) high x 160mm (6.299 in) deep.

#### 1.2.4 Environmental

The environmental specifications of the module are:

Operating Temperature: 0°C to +55°C  
Storage Temperature: -40°C to +75°C  
Humidity: <95% without condensation

#### 1.2.5 Bus Compliance

The module complies with the VMEbus Specification ANSI/IEEE STD 1014-1987, IEC 821 AND IEC 822 for a Data Transfer Bus (DTB) Slave. The standard addressing configuration is A24/A16:D16/D08 but can be upgraded to A32/A24/A16:D32/D16 by using the P2 connector. Even and odd addressing is supported for D08.

Neither SYSFAIL or interrupts are supported, but can be added by the user with jumpers to the P1 connector. IACKIN is tied directly to IACKOUT and BRX is tied directly to BGX. These configurations are easily modified by cutting accessible circuit traces.

## 2.0 INSTALLATION

### 2.1 UNPACKING AND INSPECTION

In most cases the VME Prototyping Module will have been individually sealed and packaged for shipment. Verify that there has been no damage to the shipping container. If damage exists then the container should be retained as it will provide evidence of carrier caused problems. Such problems should be reported to the carrier immediately as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and plastic bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

### 2.2 HANDLING PRECAUTIONS

The VM100 contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

### 2.3 INSTALLATION

**CAUTION: Read the entire User's Manual before proceeding with the installation and application of power.**

#### SET THE MODULE'S ADDRESS AS DESCRIBED IN

3.2. Insert the module into the appropriate slot according to the desired priority. Apply power. If no obvious problems exist, proceed to communicate with the module as outlined in Section 5.0 (Operating Instructions).

### 2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum.

The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.



## 3.0 FUNCTIONAL DESCRIPTION

### 3.1 GENERAL

A block diagram is provided on sheet 1 of the schematics in Appendix B and a layout of the board is shown in Figure 1.

#### 3.1.1 Address Decode and Data Buffer

Address decoding is performed using the upper sixteen VME A24 address bits. The bits are compared to the address select switches (S1 and S2) by the comparators at U7 and U8 (Reference schematic sheets 3 and 4). The comparator U8 produces  $UP=Q/$  when VA16 through VA23 matches the switch settings of S1. U7 produces  $LP=Q/$  when VA08 through VA15 matches the switch settings of S2. The results of the address comparisons are fed to PAL2 (U5). For further analysis, see section 4.1.2.

The 16-bit bidirectional data buffers (U1 and U2) pass the VMEbus data to and from the VM100 logic. When a valid VMEbus cycle occurs  $SEL/$  is used to enable the data buffers and determine the data direction. On a write cycle, the data buffer will enable data to flow from the VMEbus to the logic on the VM100.

#### 3.1.2 Control Logic

The control logic uses the results of the address comparators along with other VMEbus control and address signals to decode a valid VMEbus cycle to the VM100 (Ref. schematic sheet 4).

PAL2 (U5) contains the logic to: 1) determine the address mode from the S3 (ID12 and ID13) switch settings, 2) check the VMEbus address modifier bits for the proper value, 3) and provide an active low level on  $P=Q/$  if the address signals and address modifier are valid for the selected address mode. Address lines VA06 and VA07 are compared with the switches SW06 and SW07 on S3.

Example of a valid mode and address configuration:

A system with a 24-bit address range issues an address of 10FFC0h and an address modifier of 39h to a module with ID12 and ID13 set low (i.e., S3-7 and S3-8 set to the ON position), address switch S1 set to 10h (only S1-4 OFF), address switch S2 set to FFh (all OFF), and address switch S3-5 (SW06) and S3-6 (SW07) set high (both OFF). This combination will cause the  $P=Q/$  term of PAL2 (U5) to be active low while these conditions continue.

Insert VM100 Layout Here

**Figure 1. VM100 Layout**

PAL1 (U4) monitors the VMEbus control signals for a valid VMEbus cycle and P=Q/ from PAL2 (U5) to determine if the host processor is accessing this module. When a valid VME cycle is detected DSSEL/ will go active low. DSSEL/ feeds a delay line to create DLY1-3, LDTACK and DTACK\*. If DSSEL/ is still valid when DLY1 goes high, DSSEL/ will be saved in the SEL/ latch, and VA01, VA02, and VA03 will be saved in the A01, A02, and A03 latches for the duration of the cycle. DTACK\* is used to signal completion of the cycle to the host processor. The latched terms will stay latched until the host processor terminates the cycle by raising both DS0\* and DS1\* to a high level. All the VMEbus signals from connector P1 are buffered, decoded and redistributed to the module. The Data Strobes (DS0\* and DS1\*) and WR/ signals are received and buffered by PAL1 (U4).

PAL's U6 and U9 decode the low order address bits and data strobes to provide read and write control signals to the on-board logic. On a read cycle, 16-bit data transfers are always enabled. On a write cycle, one or two 8-bit data transfers are clocked. Pin 9 (RCONT) is used to distinguish between read and write cycles. If RCONT is low, a write function (WRx) is performed. On a write cycle, the leading edge of WRx is used to store data from the VME data bus into one or two register locations, while on a read cycle the READx-y/ signal enables read data to be sent to the VME data bus.

The VM100 supports D08(even/odd) capability; therefore, write data is on an 8-bit basis. 16-bit writes are accomplished by strobing two WRs simultaneously. Reads are always on a 16-bit basis and the host processor retains only the bits it requires.

### 3.1.3 Power Distribution and Connector Interfaces

The +5 volt DC power for the VM100 is supplied by the VME P1 connector at pins A32, B32, and C32. The +12 volt DC power for the module is supplied by the VMEbus P1 connector at P1-C31. Ground connections for the module are supplied at P1 pins A9, A11, A15, A17, A19, and C9.

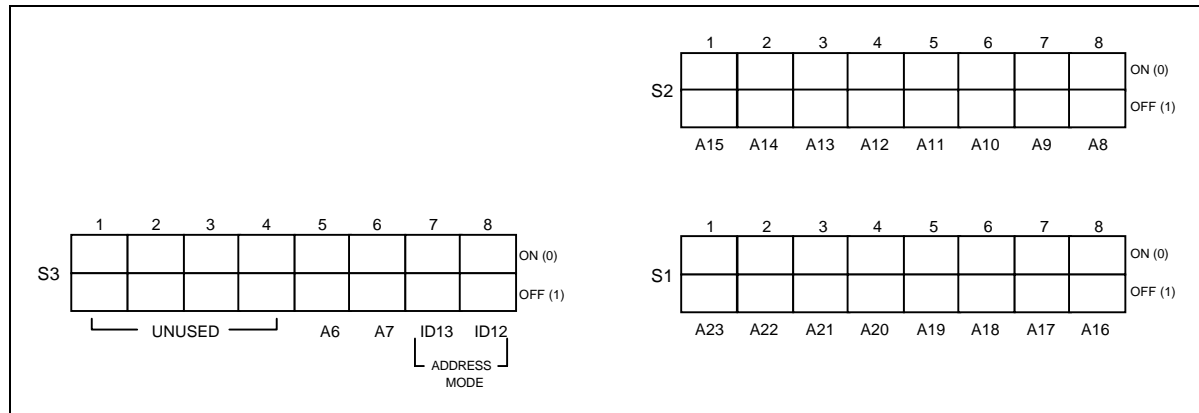
The user is supplied +5 volts and ground on power strips on the top and bottom of both sides of the module. Wire wrap post may be installed on these busses or the user may solder directly onto the bus. Similarly, +12 is available near the P1 connector.

## 3.2 CONTROL

The 8-bit select switches shown as S1, S2, and S3 in Figure 2 are used to select the VME module address. A16 and A24 address modes are available based on the configuration bits (ID12 and ID13). Refer to the operating instructions in section 4.1.1 for address switch selections.

## 3.3 INDICATORS

The VM100 has no front panel indicators.



**Figure 2. Switch Configuration**

### 3.4 CONNECTORS

The VM100 provides the P1 VMEbus connector and provisions to mount a P2 connector. No external connections are provided at the front panel, but provisions for two DIN41612 compatible connectors are available. Access to the buffered data and control signals is via solder tabs with plated through holes. The user may install wire-wrap posts in these locations or solder directly to the tabs.

### 3.5 CONFIGURATION REGISTERS

There are no configuration registers.

### 3.6 USER INTERFACE SIGNALS

The VM100 performs all the VMEbus interface functions and provides a buffered set of address, data, and control signals to the user. See Appendix A for the timing relationships of the user interface signals.

#### 3.6.1 D00 to D015

The bi-directional buffered 16-bit VME data bus, with the drive/receive characteristics of the ALS transceiver (74ALS245).

#### 3.6.2 WR0 to WR7

D00 through D15 are stable at the rising edge of WR0 thru WR7 clocks. Each write clock corresponds to an 8-bit data register. For 16-bit writes, two write clocks occur simultaneously. See Table I.

**Table I. Write Clock Address Decode**

DS1/	DS0/	A01	A02	A03	WR <sub>x</sub>	Data Written
1	0	0	0	0	WR0	D0 to D07
0	1	0	0	0	WR1	D8 to D15
1	0	1	0	0	WR2	D0 to D07
0	1	1	0	0	WR3	D8 to D15
1	0	0	1	0	WR4	D0 to D07
0	1	0	1	0	WR5	D8 to D15
1	0	1	1	0	WR6	D0 to D07
0	1	1	1	0	WR7	D8 to D15
0	0	0	0	0	WR0 & WR1	D0 to D15
0	0	1	0	0	WR2 & WR3	D0 to D15
0	0	0	1	0	WR4 & WR5	D0 to D15
0	0	1	1	0	WR6 & WR7	D0 to D15

### 3.6.3 READ0-1/ to READ6-7/

The CMOS compatible drive device generates the first eight register read gates to the VM100. The VMEbus data transceiver is configured to present the 16-bit data to the VMEbus while the read gate is low. All 16-bits of data are sent to the VMEbus (i.e. the host processor). See Table II.

### 3.6.4 LDTACK

DLY1 occurs approximately 40 nsec after a valid VMEbus cycle to this module is detected. The low order address bits (A<sub>x</sub>) and the valid address decode (SEL/) are latched. When these signals are stable, approximately 40 nsec later, Local Data Acknowledge (LDTACK) is generated. LDTACK is used by the VM100 to generate write gates. The user may use LDTACK to latch other pertinent information or for data synchronization. This signal is driven by an open-collector LS TTL compatible device with a 1K ohm pullup resistor. Both LDTACK (active-high) and LDTACK/ (active-low) are provided.

### 3.6.5 RST/

The SYSRESET\* from the VMEbus is buffered and supplied to the module as RST/. This signal is driven by an LS TTL compatible device.

**Table II. Read Gate Address Decode**

DS1/	DS0/	A01	A02	A03	READX-Y/	Data Passed
X	0	0	0	0	READ0-1/	D0 to D15
0	X	0	0	0	READ0-1/	D0 to D15
X	0	1	0	0	READ2-3/	D0 to D15
0	X	1	0	0	READ2-3/	D0 to D15
X	0	0	1	0	READ4-5/	D0 to D15
0	X	0	1	0	READ4-5/	D0 to D15
X	0	1	1	0	READ6-7/	D0 to D15
0	X	1	1	0	READ6-7/	D0 to D15

### 3.6.6 A01, A02, A03

VA01, VA02, and VA03 are latched into CMOS compatible drive devices on the leading edge of DLY1 and maintained until both data strobes have been negated. This insures the address will stay stable until the VMEbus cycle is complete.

### 3.6.7 SEL/

The VA08 thru VA24 address match signal is latched into CMOS compatible drive device on the leading edge of DLY1 and maintained until both data strobes have been negated. This insures the address will stay stable until the VMEbus cycle is complete.

### 3.6.8 WR/

WRITE\* from the VMEbus is buffered, using CMOS compatible drive logic to produce WR/. This signal is used to control the direction of data flow to and from the VMEbus. The read gates (READx-y) and write clocks (WRx), are a function of this signal, but it is also provided in case the user needs other forms of read/write signals.

### 3.6.9 DS0/, DS1/

These data strobes are used by the VM100 to reset the latched address signals, determine valid VMEbus cycles, and to decode the write clock signals. The data strobes are provided to the user with CMOS compatible drive logic for additional decode or timing applications.

### 3.6.10 UUP=Q/

This input to PAL2 (U5) can be used to decode the upper eight address bits to accommodate 32-bit addressing capability. This line is normally connected to ground and must be cut at J2 if it is to be used.

### 3.6.11 VCC, GND

VCC and GND strips are provided at the top and bottom of the board. These strips have 0.1 inch spaced holes into which wire-wrap post may be installed or wires soldered.



## 4.0 OPERATING INSTRUCTIONS

### 4.1 NORMAL OPERATION

The VM100 performs the VMEbus interface functions and provides the user with a simplified set of control and data signals. The VMEbus interface section contains switch selectable address mode and address decode logic, along with an address modifier monitor and proper timing for DTACK\*.

For immediate use of the VM100, simply configure the address mode and module address, insert the module in a VME chassis and perform a read or write command. The resultant read data is from a pull-up TTL input and will most likely be all ones. Write data to this module only goes to the user output pins, but may be considered successful if a Bus Error does not occur.

Additional information concerning application and connections of the VME Prototyping Modules may be found in Application Notes from C&H. (Dwg. No. 11026161).

#### 4.1.1 Address Switch Selection

The VM100 board select (SEL/) is a function of the address mode select switches (S3), the address select switches (S1 and S2), and the VME host address modifier code. The address mode switches (ID12 and ID13) determine the address ranges (A16 or A24) and the address modifier codes that must be valid to access the VM100. See 3 for valid address modes, address modifiers and address ranges.

When the address modifier bits coincide with the address mode selected, the VME address bits will be compared with the module address selection switches (S1 thru S3) and a signal to the control logic will flag a valid address decode. Only those addresses that are appropriate to the address mode selected are used by the address decode logic. The VM100 has an address scope of 64 registers although not all 64 are readily addressable without additional user logic.

#### 4.1.2 VME Control of Module

During a valid VME read/write cycle, when the address modifier code coincides with the address mode selected and the VME address coincides with the address selected, the VME host processor may access the VM100. Of the 64 addressable registers available to the VME processor only 16 are conceivably usable. Address lines VA01 to VA03 are latched and buffered to the user if additional registers are required, additional circuitry must be added.

### 4.2 SOFTWARE DRIVERS

No software drivers for the VME Prototyping module are supplied. The software drivers are application dependent and should be designed for the user hardware.

**Table III. Address Mode Selection Functions**

ID13	ID12	ADDRESS MODE	VALID AM	VALID MODULE ADDRESS RANGE VA31 thru VA00 (see notes)
OFF (1)	OFF (1)	A16 ONLY	29 2D	XXXX0000 through XXXXFFC0
ON (0)	ON (0)	A16/A24	29 2D and 39 3A 3B 3D 3E 3F	XXXX0000 through XXXXFFC0  and  XX000000 thru XXFFFFFFC0
<p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>1. These are the possible address ranges of the module. Consult your system memory mapping to find a suitable address range.</li> <li>2. The 16-bit address range is always enabled.</li> <li>3. AM = Address Modifiers.</li> </ol>				

## **5.0 MAINTENANCE**

### **5.1 BUILT IN TEST AND DIAGNOSTICS**

No built in test functions are provided for the VM100. The user may design in test capabilities and provide their own selftest functions.

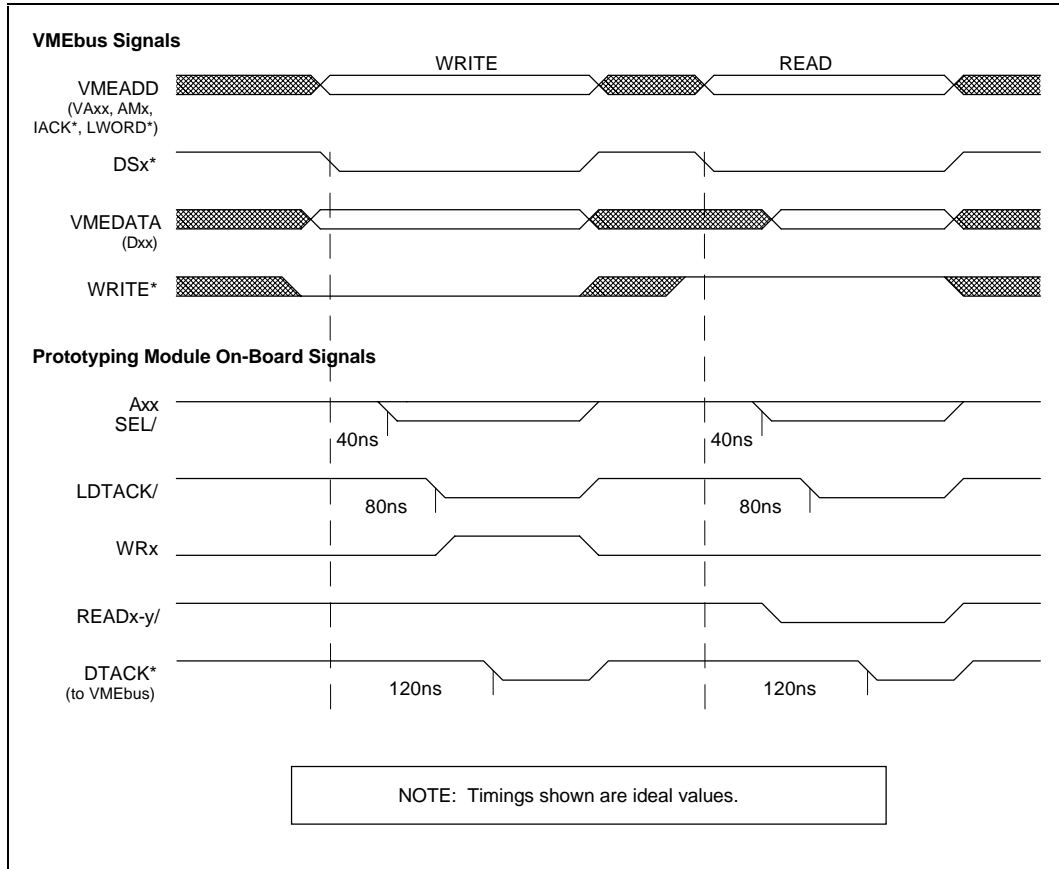
### **5.2 TROUBLE ANALYSIS GUIDE**

The first approach to trouble shooting the VM100 should be to try a VMEbus access. A successful access (read or write) will not produce a bus error. The probable cause of a bus error is the address or mode switches improperly set for system access type. A remedy for a bus error is to check the module switch settings for address and mode switches for address size setting. Also check the program for proper address and size.

Without additional circuitry, any further tests are beyond the scope of this manual.



## APPENDIX A - ELECTRICAL AND TIMING SPECIFICATION



**Figure A-1. User Signal Timing**



## **APPENDIX B - SCHEMATICS**

The following pages contain the schematics for the VM100.



















**NOTES:**



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