USER'S MANUAL

VXI
MIL-STD-1553B
BUS ANALYZER/
SIMULATOR

MODEL
VX480B

Manual Part No: 11026404A

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INTRODUCTION

This manual describes the functional operation of the C&H Model VX480B VXI 1553 module (Part No. 11026400). This module is one of a number of test and data acquisition/control modules in the VME and VXI format provided by C&H.

Contained within this manual is information on the physical and electrical specifications, installation and startup procedures, operating procedures, functional analysis, and figures and diagrams required to adequately support this product.

The part numbers covered by this manual are:

Part Number	Description
11026400-0001	VX480B with Triax front panel connectors
11026400-0002	VX480B with 9-pin Dsub front panel connector

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1.0 GENERAL DESCRIPTION

The VX480B provides Bus Controller/Multi-Remote Terminal functions on a B-Size VXI module. The VXIbus interface is dual access, allowing the host to update data resident memory on the card even when the interface is active. This capability allows support of full dynamic simulation.

1.1 PURPOSE OF EQUIPMENT

The VX480B connects the dual redundant backup channels to the P2 VXI Local Bus for simulation systems and to externally routed connectors.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Specifications

- MIL-STD-1553B Notice II Dual Redundant Data Buses
- Customization is possible using flexible microprocessor based design
- 96K Bytes of dual ported RAM
- Standard VXI interrupts supporting fully dynamic simulation
- Direct and transformer coupled connections provided
- Complete self-test capability
- Bus Controller Mode (BC):
  - Flexible linked list structure
  - Six sawtooth functions
  - Time tagging
  - Checksum function
  - Dynamic tagging
  - Inter-message gap programmable from 20µs to 32767ms
  - Error detection
- Multiple Remote Terminal Mode (MRT):
  - Simulation of all 31 remote terminal addresses
  - Mode, broadcast and RT to RT command handling
  - Automatic operation of broadcast command received bit
  - RTs not simulated can be monitored
  - 5 µs response time
  - Six sawtooth functions
  - Time tagging
  - Checksum function
  - Dynamic tagging
  - Error detection
- Buffered MRT Mode (BMRT):
  - Received data stored in buffers
  - All standard MRT functionality

1.2.2 Electrical

The module internally uses +5V and ±12V. The power requirements are as follows:

+ 5 V	3.0A max.
+ 12 V	0.8A max.
- 12 V	0.1A max.

1.2.3 Mechanical

The mechanical dimensions of the module is in conformance with the VXI bus specification for single slot Size-B modules. The nominal dimensions are 233.35 mm (9.187 in) high x 160 mm (6.299 in) deep. The module is designed for a mainframe with 20.32 mm (0.8 in) spacing between slots. As required by the VXI bus specification, these dimensions are in accordance with those given in the VME bus specification (Rev. C.1).

1.2.4 Environmental

The environmental specifications of the module are:

Operating Temperature:	0°C to +55°C
Storage Temperature:	-40°C to +75°C
Humidity:	<95% without condensation

The cooling requirements are:

Power Dissipation:	15.50 Watts per slot
ΔPressure across module:	0.04 mm H_2O
Air Flow:	1.24 liters/second for 10°C internal temprature rise

1.2.5 Bus Compliance

The module complies with the VXIbus Specification Revision 1.4 for B-size register based modules and with VMEbus Specification ANSI/IEEE STD 1014-1987, IEC 821 and IEC 822.

Manufacturer ID:	$FC1_{16}$
Model Code:	FFC_{16}
Addressing:	A16, A24, A32
Data Transfer:	D16
Interrupts:	ROAK
Local Bus:	Class 4 Analog Medium (if jumpers installed)

2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

In most cases the VX480B will have been individually sealed and packaged for shipment. Verify that there has been no damage to the shipping container. If damage exists then the container should be retained as it will provide evidence of carrier caused problems. Such problems should be reported to the carrier immediately as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and plastic bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The VX480B contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION

> CAUTION: Read the entire User's Manual before proceeding with the installation and application of power.

Set or verify the module's logical address. Insert the module into the appropriate slot according to the desired priority. Apply power. If no obvious problems exist, proceed to communicate with the module as outlined in your host processor's user's guide.

2.4 PREPARATION FOR RESHIPMENT

If the VX480B is to be shipped separately it should be enclosed in a suitable water and vapor proof plastic bag. Heat seal or tape the plastic bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum.

The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the VX480B was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

3.0 FUNCTIONAL DESCRIPTION

3.1 GENERAL

The VX480B is a full-featured, high performance MIL-STD-1553B Serial Bus Simulator/Analyzer designed for the VXIbus backplane. The module uses a flexible microprocessor based architecture that occupies 128K bytes of offset memory. The offset memory is split into two parts. All memory is accessed as 16-bit words, however, only the lower byte is valid for the upper 64K bytes of memory. The module supports A24 and A32 addressing modes with D16 data transfer capabilities. The interrupt level and status/ID are fully programmable.

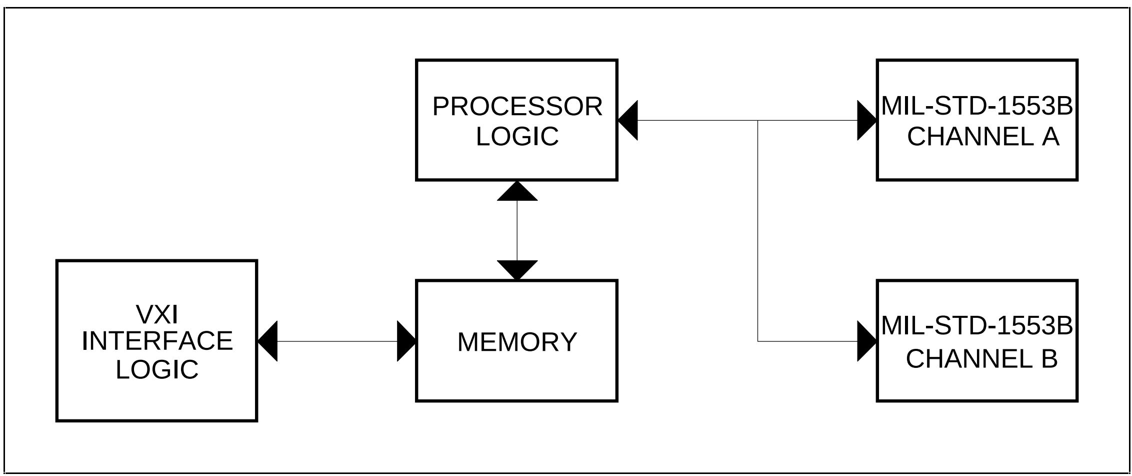


Figure 1. Simplified Block Diagram

3.2 SWITCHES AND JUMPERS

Several switches and jumpers are provided for configuring the VX480B. The location of the switches are shown in Figure 2 and their functions are described below.

3.2.1 Logical Address Switches

An 8-bit Logical Address Switch is provided to uniquely identify the module in the system. See 4.0 for setting instructions.

3.2.2 A24 / A32 Address Mode Jumper

A jumper (J2) is provided to allow the user to select A24 addressing (jumper link in) or A32 addressing (jumper link out).

3.2.3 1553 Bus Configuration Jumpers

Jumpers are provided to configure Bus A and/or Bus B as direct coupled or transformer coupled, to route the signals to the local bus (P2 connector) or to the front panel Triax connectors (or optional 9-pin DSUB connector), and to select the polarity of the signals. The location of the jumper are shown in Figure 2.

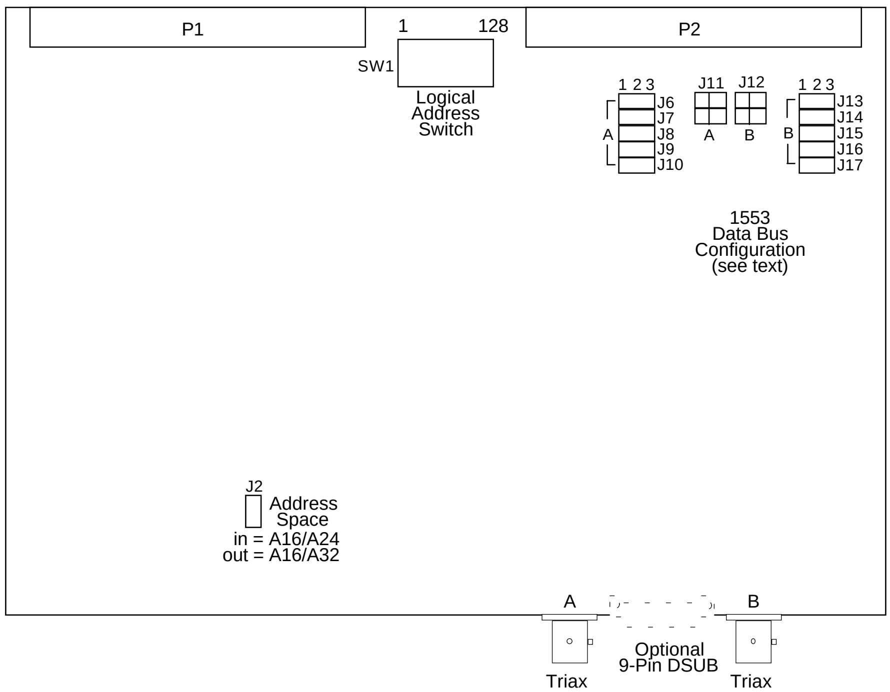


Figure 2. Location of Switches and Jumpers

3.2.3.1 Bus Coupling Configuration

Table I shows the jumper arrangement required to configure the bus coupling method for direct or transformer coupling.

Table I. 1553 Coupling Configuration

Function	Bus A		Bus B	
Direct coupled	J6	1-2	J13	1-2
	J7	1-2	J14	1-2
Transformer coupled	J6	2-3	J13	2-3
	J7	2-3	J14	2-3

3.2.3.2 Bus Signal Routing Configuration

Table II shows the jumper arrangement required to route the 1553 bus signals to the P2 Local Bus or to the front panel BJ77 Triax connectors or to the optional 9-pin DSUB connector.

Table II. 1553 Signal Routing Configuration

Function	Bus A		Bus B	
Route signals to the Front Panel Triax connectors (or optional 9-pin DSUB)	J8 J9 J10	1-2 1-2 1-2	J15 J16 J17	1-2 1-2 1-2
Route signals to the P2 Local Bus	J8 J9 J10	2-3 2-3 2-3	J15 J16 J17	2-3 2-3 2-3

3.2.3.3 Bus Polarity Select Jumpers

Jumper pairs (J11 and J12) are provided to select the polarity of the 1553 bus signals at the local bus and front panel connectors. Theses jumpers are normally used by the factory to configure the board for alternate transformer configurations, however, the may also be used to reverse the polarity for diagnosing or correcting a system level wiring problem. The factory default setting provides polarity in accordance with Mil-Std-1553B Notice II (i.e., positive Manchester level connected to the center pin). To reverse the polarity, change the jumpers from 1-2 and 3-4 to 1-4 and 2-3, or vice versa.

3.3 INDICATORS

Two LED indicators are provided on the front panel. One indicates access to the MODID, the other indicates the BOARD SELECT status.

MODID: This red front panel LED illuminates whenever the host processor applies the MODID signal to the slot the module is occupying.

BD SEL: This green front panel LED illuminates whenever the module is properly accessed by the host processor.

3.4 CONNECTORS

See Appendix B for pin configurations.

3.4.1 Front Panel Connectors

Two BJ77 Triax connectors (or optionally two 9-pin DSUB connectors) are provided for 1553 Bus A and Bus B connection. The connectors can be configured for either direct or transformer coupled. See 3.2.3 and 3.2 for jumper configurations.

3.4.2 Rear Connectors

3.4.2.1 P1 Connector

The P1 connector is configured in accordance with the VXI P1 specification.

3.4.2.2 P2 Connector

The P2 connector is configured in accordance with the VXI P2 specification with utilization of the local bus for 1553 data. Bus A and Bus B direct and transformer lines can be connected to the local bus using the jumpers discussed in 3.2.3. If the jumpers are configured to use the local bus, then the line is connected to both row 'A' and 'C' of the local bus. If the local bus is not used for 1553 communication, then row 'A' and 'C' are shorted as specified in the VXI specification.

3.5 CONFIGURATION REGISTERS

There are two types of registers used to configure and control the VX480B. VXI compliant control registers are used to control and status the VXI interface and are located in the A16 address space according to the logical address. 1553 control registers are located in the A24 or A32 address space at a base address specified in the VXI Offset register.

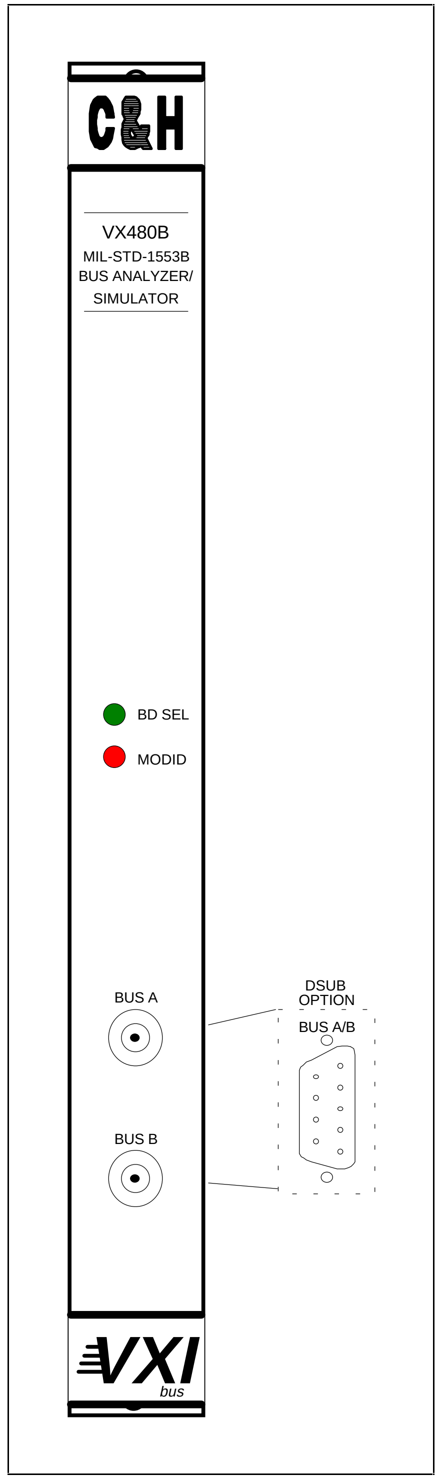


Figure 3. Front Panel

3.5.1 VXI Configuration Registers

The VXI configuration registers contain basic information needed to configure a VXIbus system. The configuration information includes: manufacturer identification, product model code, device type, memory requirements, device status, and device control. The registers are briefly described below and are detailed in Figure 4:

> VXI Identification (ID) Register (0000h) - A read of this registers provides manufacturer identification, device classification (i.e., Register Based), and the addressing mode (A16/A24/A32). A write to this register has no effect.
>
> VXI Device Type Register (0002h) - A read of this register provides the model code identifier and the amount of memory required. A write to this register has no effect.
>
> VXI Status/Control Register (0004h) - A read of this register provides the state of the A24/A32 Enable bit, the state of P2 MODID* line, and the Ready and self-test Passed status. A write of this register controls the enable/disable of A24/A32 addressing and can reset the module.
>
> VXI Offset Register (0006h) - This read/write register defines the base address (OFFSET) of the 1553 configuration registers and memory as shown below.

bit	31 24	23 17	16 15 0
A24		A24 Offset	Reg/Memory Address
A32	A32 Offset (MSB)	A32 Offset (LSB)	Reg/Memory Address

Table III. VXI Register Address Map

A16 Address	Description
0008-001F	Unused Registers Locations
0006	VXI Offset Register
0004	VXI Status Register
0002	VXI Device Type Register
0000	VXI Identification (ID) Register

00	VXI ID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								Not Used							
Read	Device Class		Address Space		Manufacturer ID											

Device Class ⇒ Device Class (Register Based = binary 11)
Address Space ⇒ Address Space (00 = A16/A24, 01 = A16/A32)
Manuf. ID ⇒ Manufacturer Identification (C & H Technologies = $FC1_{16}$)

02	VXI DEVICE TYPE															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used															
Read	Req'd Memory				Model Code											

Req'd Memory ⇒ Amount of memory required by card (128Kbytes - in A24 addressing mode = 0110, in A32 addressing mode = 1110)
Model Code ⇒ Model code (C&H Model VX480B = FFC_{16})

04	VXI Status/Control															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	A24 A32 Ena	Not Used														Rst
Read	A24 A32 Act	MOD ID*	Not Used										Rdy	Pass	0	0

A24/A32 Ena ⇒ Enable A24/A32 Access (1 = enabled)
Rst ⇒ Reset (1 = reset card)
A24/A32 Act ⇒ A24/A32 Active (1 = A24 or A32 addressing is active)
MOD ID* ⇒ Module ID Status (0 = P2 MODID line is selected)
Rdy ⇒ Ready (1 = ready)
Pass ⇒ Self-test pass/fail indicator (0 = executing or failed, 1 = passed)

06	VXI OFFSET REGISTER															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	A24 Offset/A32 Offset (MSB)							A32 Offset (LSB)								N/U
Read	A24 Offset/A32 Offset (MSB)							A32 Offset (LSB)								0

A24/A32 Offset ⇒ Most significant bits of A24 and A32 (upper part) offset address
A32 Offset ⇒ Least significant bits of A32 offset address (lower part)
N/U ⇒ Not Used (ignored)

Figure 4. VXI Configuration Registers

3.5.2 1553 Common Configuration Registers Description

Time Stamp Register (Offset + FFFE) - This register is a read/write location that gives the host access to the time stamp. The time stamp format is per MIL-STD-1760A. The host computer can read all 16-bits of the register with bit 0 representing 64µs. However, this bit is not transmitted on the 1553 bus, effectively resulting in a 128µs time stamp. When a time stamp word is transmitted, bit 0 is always zero.

Table IV. Common MIL-STD-1553 Registers

Addr (Hex)	Description
Offset + FFFE	Time Stamp (read/write)
Offset + FFFC	RESERVED
Offset + FFFA	Amplitude (write only)
Offset + FFF8	RESERVED
Offset + FFF6	1553 Control (read/write)
Offset + FFF4	1553 Status (read only)
Offset + FFF2	IRQ Level/Status ID (read/write)

Amplitude Register (Offset + FFFA) - The amplitude register is a write only location used by the host to control the amplitude of the bus signals transmitted by the interface. With direct coupling and a bus load of 70 ohms, the amplitude can be varied from 0 volts with a value of zero to approximately 10 volts with a value of FF_{16}.

1553 Control Register (Offset + FFF6) - The control register is a read/write location used by the host to determine the operation and operational mode of the interface. The interface remains inactive until the G/H bit is set. When G/H is set, the interface examines the BMRT, ST and B/R bits to determine the operational mode according to the following table.

bit 3	2	1	Mode
0	0	0	Multiple Remote Terminal (MRT)
X	0	1	Bus Controller (BC)
X	1	X	Selftest
1	0	0	Buffered Multiple Remote Terminal (BMRT)

Note: To insure proper operation, first set the mode then set the G/H bit with same mode. Do not change the operational mode while the interface shows busy because erroneous actions may result. Instead, clear the G/H bit, change the mode, then set the G/H bit.

1553 Status Register (Offset + FFF4) - The status register is a read only register used by the host to discover the current state of the interface.

IRQ Level/Status Register (Offset + FFF2) - The IRQ level/status register defines the interrupt request level and base status used when the interface generates a VXI interrupt. An IRQ level of zero disables interrupts. When an interrupt is generated, the folowing value is added to the base status:

Interrupt Source	Value Added
Selftest completion	2
BC operation	2
BMRT command received	0

During an interrupt acknowledge cycle, the logical address is presented in the lower byte and the status value is presented in the upper byte.

3.5.3 Bus Controller Registers

Step Registers (Offset + FFE6) - There are six step registers (STEP 0 to STEP 5) starting at this location and progressing downward. When used with the flag codes, they are used as additive step values.

Count Register (Offset + FFE4) - The count register is used to determine the number of iterations a list of messages is to be transmitted. When the end of the list is reached, the count is decremented. When the count is decremented to zero, the interface is returned to a quiescent state. If the count is initially set to zero when Bus Controller mode is entered, then the list of messages is transmitted continuously until the interface is halted by the G/H bit in the control register. If interrupts are enabled, an interrupt is generated at the completion of the number of iterations. If transmitting continuously no interrupt is generated until BC mode is stopped.

Root Register (Offset + FFE2) - The root register contains the address of the first message to be transmitted when transmission commences. When the end of the list of messages is reached, this register is used to refresh the list of messages.

Note: The value entered in the Root Register must be scaled for the on-board processor. This is done by dividing the address by two.

3.5.4 Remote Terminal Registers

Step Registers (Offset + FFE6) - There are six step registers (STEP 0 to STEP 5) starting at this location and progressing downward. When used with the flag codes, they are used as additive step values.

RT Status Registers (Offset + FFE4) - There are 31 status registers, one for each Remote Terminal supported by the interface. They begin at this location and progress downward. The status word register contains the pattern of bits for the status word to be transmitted by the terminal on receipt of a valid command. The RT Enable/Mask byte is located $10001 above each of the status registers. This byte is used to enable/disable the RT and to specify the dynamic tag mask.

3.5.5 Buffered MRT Registers

The Buffered Remote Terminal registers are identical to MRT mode with the exception of the RX Data Pointer is referred to as the RX Buffer Pointer.

3.5.6 Self-test Registers

After the self test Built In Tests have been completed the busy bit in the status register will be cleared. The results of the BIT can then be found in the result register while the firmware version and revision can be found in the version and revision registers.

Results Register (Offset + FFF0) - Contains the results of the self test operation. If this register is zero then all the tests have passed and the interface is functioning normally, if the register is not zero then one or more tests have failed. Refer to 4.5 for the meaning each bit.

Version Register (Offset + FFEE) - Contains the version of the firmware currently running the on-board processor.

Revision Register (Offset + FFEC) - Contains the revision of the firmware currently running the on-board processor.

Offset +FFFE	Time Stamp															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Time Stamp Value (see text)															
Read	Time Stamp Value (see text)															

Offset +FFFA	Amplitude															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used							Bus Signal Amplitude ($FF ≈ 10 Volts)								

Offset + FFF6	1553 Control															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used												MD	ST	B/R	G/H
Read	Not Used												MD	ST	B/R	G/H

MD ⇒ Mode, (0=MRT, 1=BMRT)
ST ⇒ Self-Test (1 = perform BIT, 0 = normal operation)
B/R ⇒ Bus Controller (BC)/Remote Terminal (RT) Mode Select (1 = BC, 0 = RT)
G/H⇒ Go/Halt Flag (0 = halt, 1 = go)

Offset + FFF4	1553 Status															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	Not Used															BSY

BSY ⇒ Busy (1 = busy)

Offset + FFF2	Interrupt Request Level/Status															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Level								Base Status							
Read	Level								Base Status + Interrupt Source							

Level ⇒ Interrupt Request Level (0 = interrupts disabled)
Status ⇒ Interrupt Source (see text)

Figure 5. 1553 Common Configuration Registers

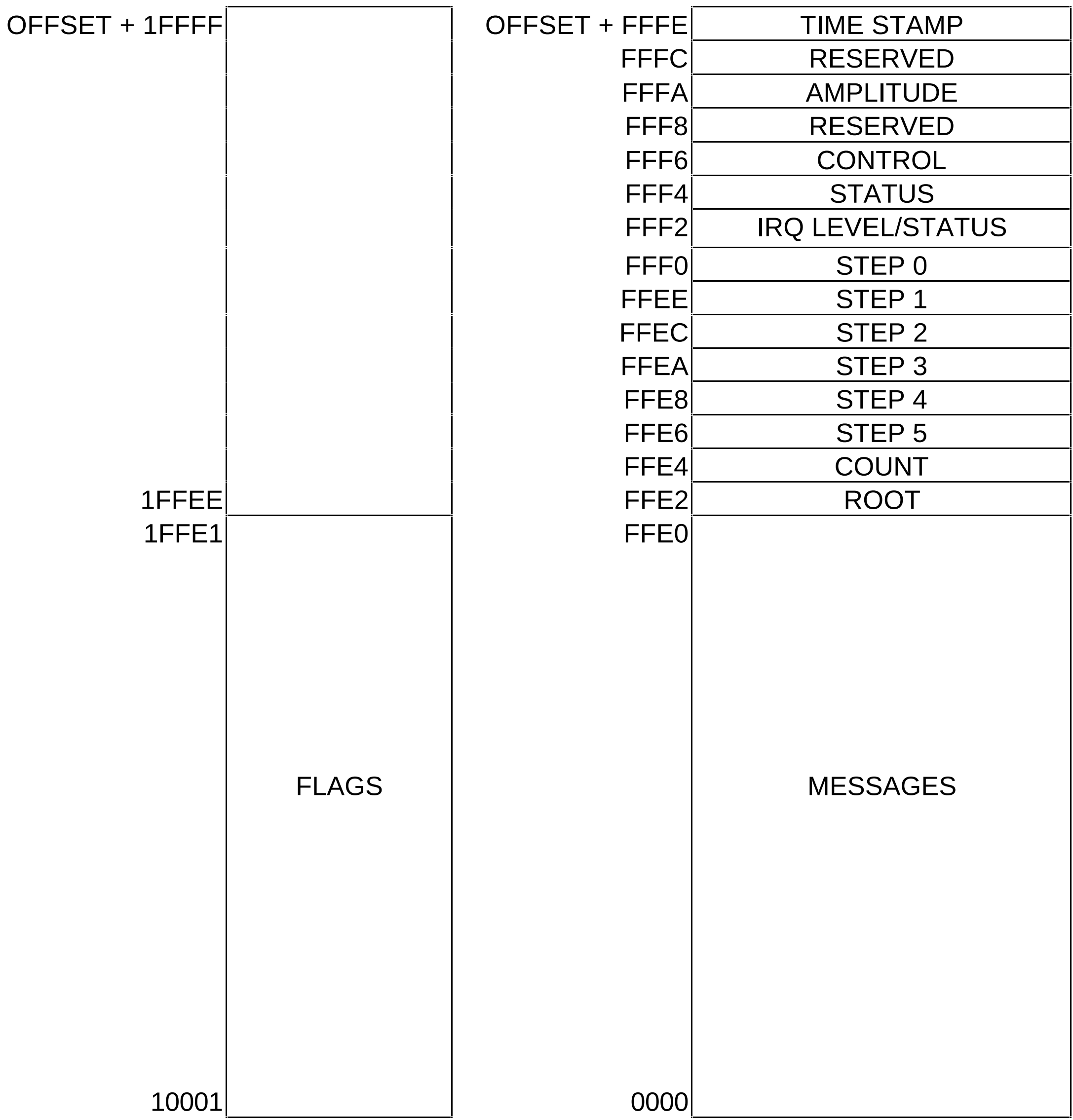


Figure 6. Bus Controller Memory Map

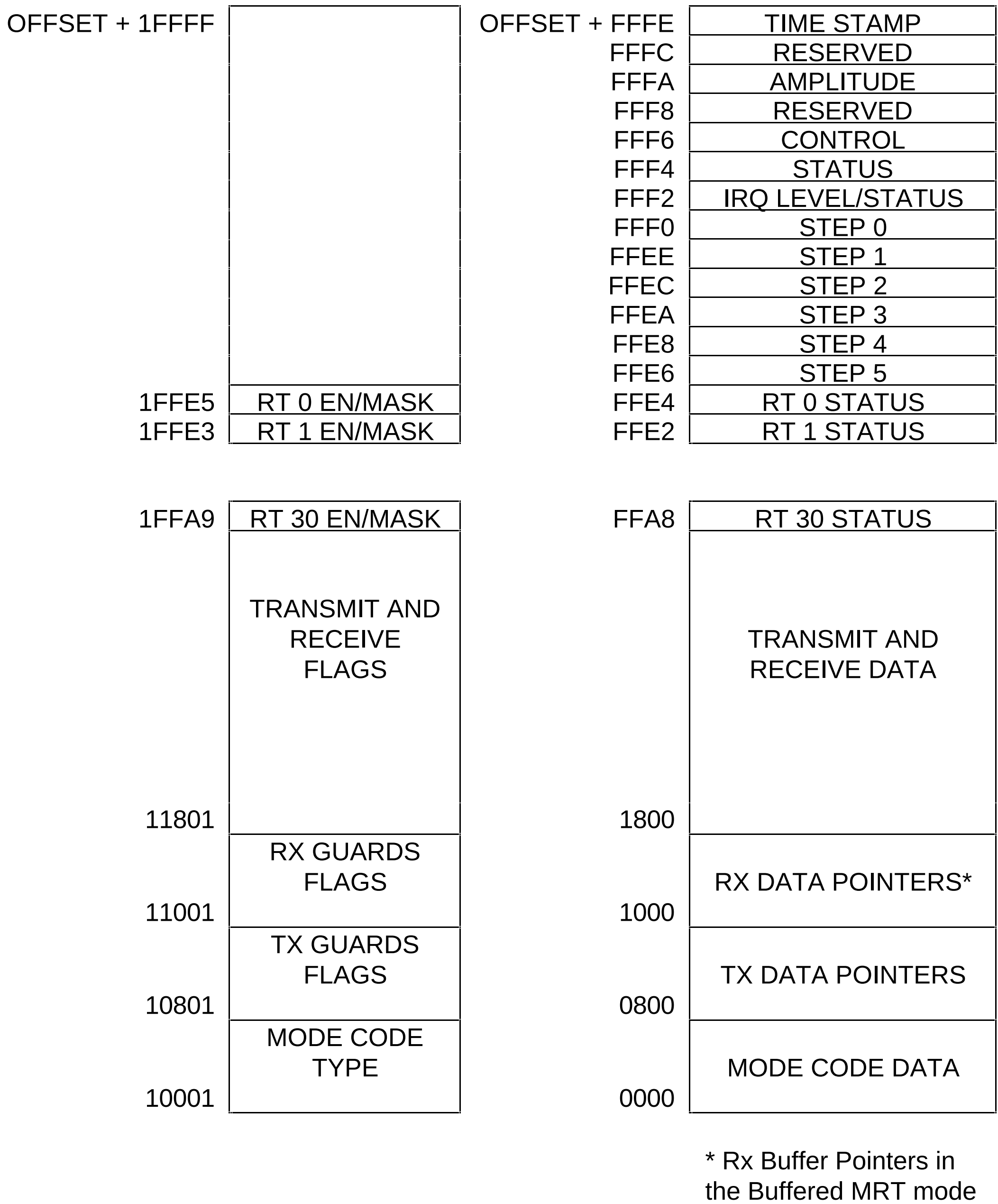


Figure 7. Remote Terminal Memory Map

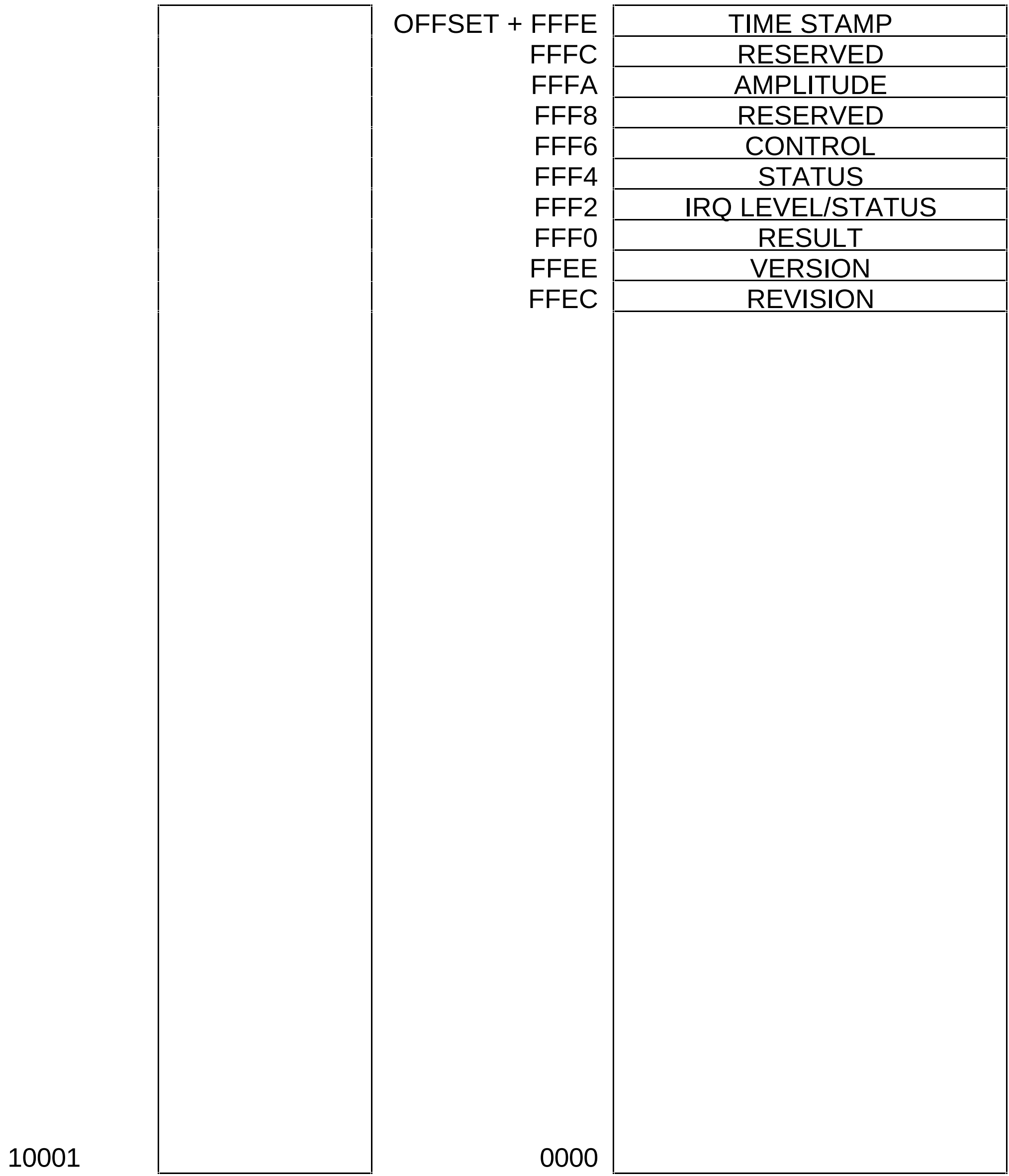


Figure 8. Self-test Memory Map

4.0 OPERATING INSTRUCTIONS

4.1 NORMAL OPERATION

Prior to installation, the module's logical address must be set. The logical address has a range of 0 to 255. Any value within this range is valid, but care should be taken not to set the logical address the same as another module in the system. Position 1 on the switch is the most significant bit and has a weighted value of 128 when the switch is in the off position. Position 8 on the switch is the least significant bit and has a weighted value of 1 when the switch is in the off position. The sum of the weighted values of all the switches in the off position is the module's logical address. The VXI secondary address is the logical address divided by 8.

4.2 BUS CONTROLLER OPERATION

Each message transmitted by the Bus Controller uses a message structure consisting of a header and a variable data section. The message header describes where the data can be found, the word count, the inter-message gap, and the command word. Message headers are linked using pointers. The message data can immediately follow the header or be pointed to using a data pointer (see Figure 9). Additional control information, one byte wide, is located $10001 above the header or data.

4.2.1 Forward Link

This word contains pointer to the next message to be transmitted. A null pointer is used to mark the end of the list. The value entered for the forward link address must be scaled for the on board microprocessor. This is done by right shifting the least significant 16 bits of the address by one place. The most significant bit of this word will indicate whether the data block of the message pointed to directly follows the command word (see Figure 10) or is accessed via a pointer (see Figure 11). If the most significant bit is 0 the data follows the command word. If it is 1 the data is accessed via a pointer.

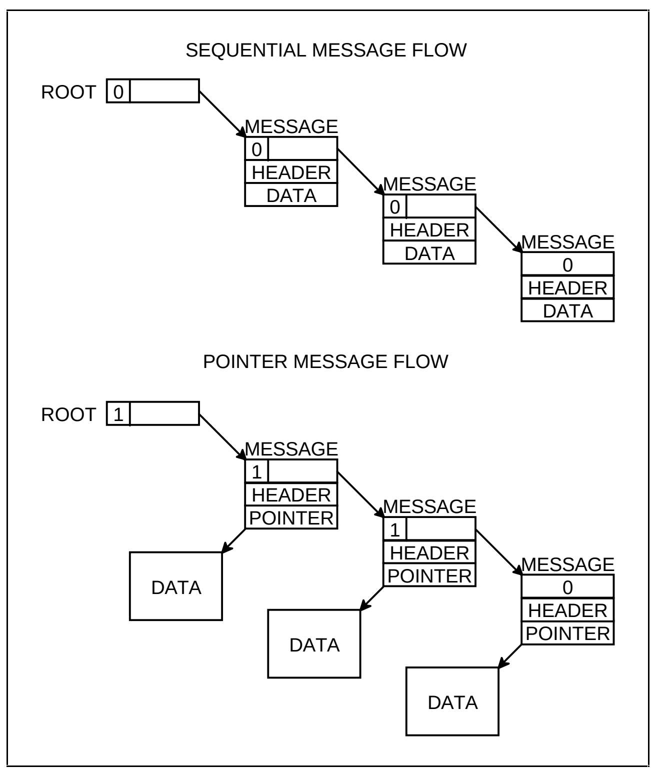


Figure 9. Bus Controller Message Flow

4.2.2 RT-RT Flag + Tx Word Count

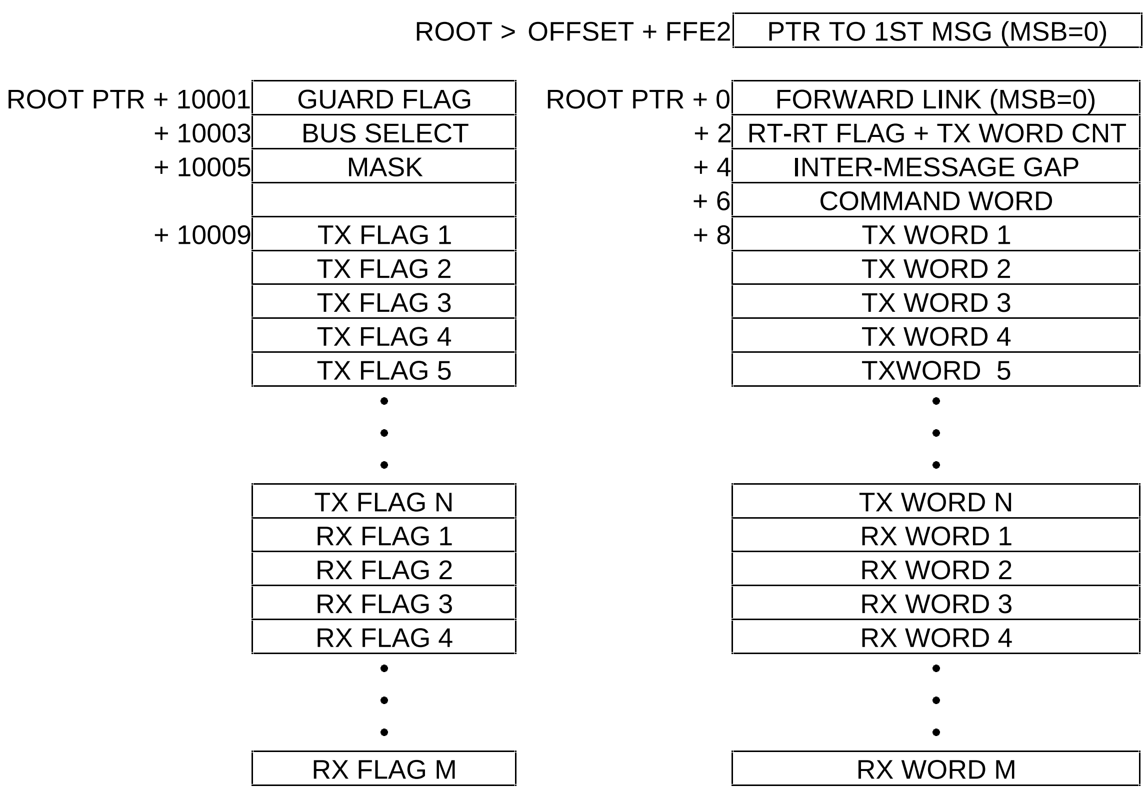
This word contains a count of the words to be transmitted. This count excludes the command word itself. If the message is an

RT to RT transfer the count must be one to enable the second command word to be transmitted and the most significant bit of the word must be set. The byte located $10000 above this word is the Bus Select byte and is used to select which bus the associated command shall be transmitted. Bus A is selected by setting the byte to the value of $DE. Bus B is selected by setting it to $FD.

4.2.3 Inter-message Gap

This inter-message gap for the message. If the most significant bit in this location is set then the duration is in milliseconds else the time is in microseconds. This gives a range of inter-message gaps from the minimum to 32767 microseconds in 1 microsecond increments and 1 to 32767 milliseconds in 1 millisecond increments.

Note: In broadcast mode there is a -7 microsecond offset.



where N = Tx Word Count
M = Number of words expected according to the command word

Figure 10. Bus Controller Sequential Message Format

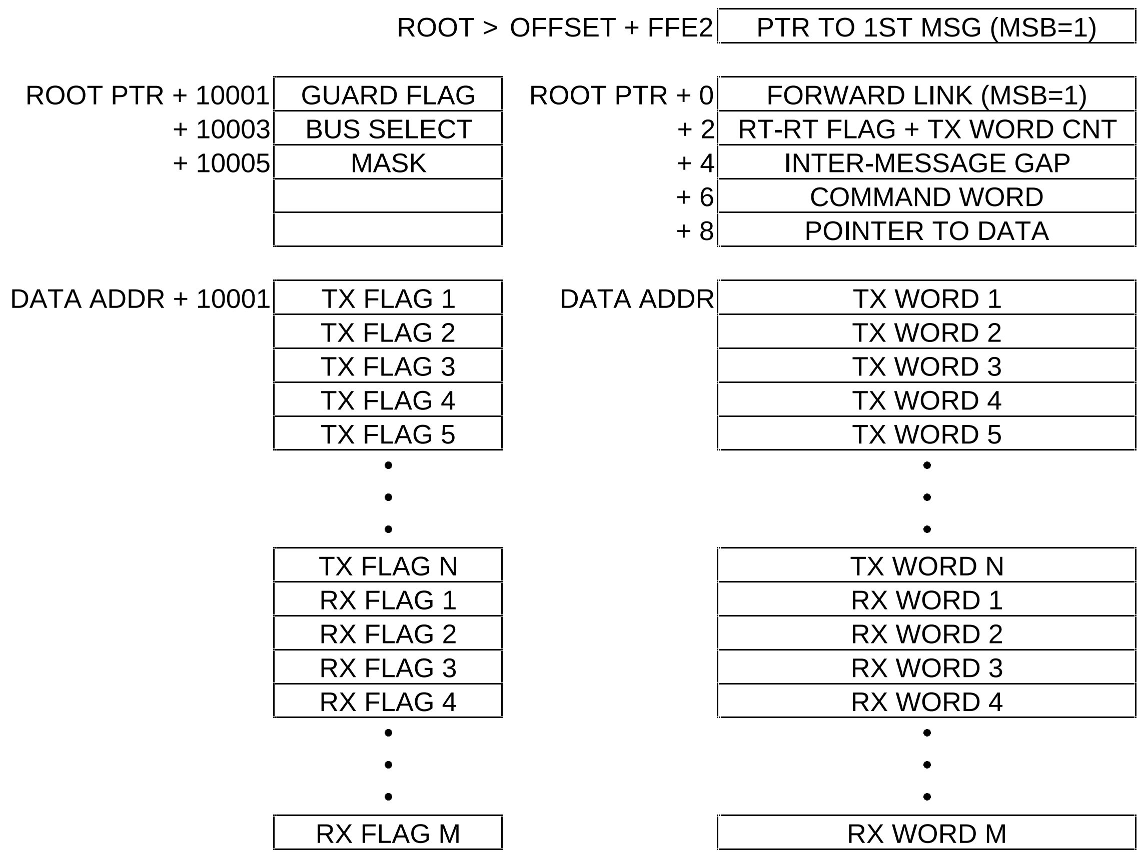


Figure 11. Bus Controller Pointer Message Format

4.2.4 Command Word

This word contains the MIL-STD-1553 command word for the message.

4.2.5 Guard Flag

The guard flag byte is set to non-zero when the message data is being accessed. This flag can be used by the host to help ensure data integrity.

4.2.6 Bus Select

The Bus Select byte is used to select which bus the associated command is transmitted. Bus A is selected by setting the byte to the value of $DE. Bus B is selected by setting it to $FD.

4.2.7 Mask

The mask byte used in conjunction with a dynamic tag word and its associated flag code. Based on the flag code, the value of the mask is used to determine which bits in the data word are the source identification code and which bits are the dynamic counter code. The table below defines how the mask is used:

Flag Code	Mask Defines Usage of	Source Identification Code	Dynamic Counter Code
$D8-$E2	Lower byte	Bits 8-15 and the 0 bits in mask	1 bits in mask
$E4-$EE	Upper byte	0 bits in mask	Bits 0-7 and the 1 bits in mask

4.2.8 Pointer To Data

This word contains a pointer to the message data. If the most significant bit of the forward link to the message is 1 then this pointer is required to indicate the address of the first data word. This enables more than one message to use the same data. If the most significant bit of the forward link to the message is 0 then the pointer is not required, the command word is followed by the first data word.

Note: The value entered in the pointer locations must be scaled for the on-board processor. This is done by dividing the address by two.

4.2.9 Transmit (Tx) Words

The Transmit Words are transmitted with the command if the T/R bit is zero. The contents of the data words transmitted can be modified by setting the flag byte, located $10001 above the data word, to one of the following flag codes:

Flag Code	Description
$D8	Dynamic tag word, dynamic counter not above bit 7, step 0
$DA	Dynamic tag word, dynamic counter not above bit 7, step 1
$DC	Dynamic tag word, dynamic counter not above bit 7, step 2
$DE	Dynamic tag word, dynamic counter not above bit 7, step 3
$E0	Dynamic tag word, dynamic counter complement of $D8 counter with carry
$E2	Dynamic tag word, dynamic counter complement of $D8 counter
$E4	Dynamic tag word, dynamic counter above bit 7, step 0
$E6	Dynamic tag word, dynamic counter above bit 7, step 1
$E8	Dynamic tag word, dynamic counter above bit 7, step 2
$EA	Dynamic tag word, dynamic counter above bit 7, step 3
$EC	Dynamic tag word, dynamic counter complement of $E4 counter with carry
$EE	Dynamic tag word, dynamic counter complement of $E4 counter
$F8	Check Sum
$F9	Time Stamp
$FA	Step 5 }
$FB	Step 4 }
$FC	Step 3 } Sawtooth
$FD	Step 2 }
$FE	Step 1 }
$FF	Step 0 }

4.2.9.1 Dynamic Tag Words

Dynamic tag words consist of a source identification code and a dynamic counter code which increments each time the word is transmitted. Based on the flag code, the value of the mask is used to determine which bits in the data word are the source identification code and which bits are the dynamic counter code. See 4.2.7 for a definition of the mask.

<u>Codes $D8 to $DE</u>

These codes are used when the dynamic counter code does not extend above bit 7 of the data word. They are used in conjunction with the mask where those bits which are occupied by the dynamic counter code are set to one. For example, if it is required that bits 0 to 3 of the dynamic tag word contain the dynamic counter code and bits 4 to 15 the source identification code, then the mask should be $OF.

The step sizes used by the dynamic counters are defined in the same way as the normal sawtooth functions. The source identification code and counter start value are set in the data word to which the flag is assigned. For example, if flag code $D8 is associated with data word $1280 with the mask set to $3F and step 0 set to $0001 then the first time it is transmitted $1280 will be sent, the next time $1281 and so on.

If it is required that the dynamic counter not start at bit 0, the step size should be set to a power of 2 (i.e., if the counter is required to start at bit 2, set the step size to $0004).

<u>Codes $E4 to $EA</u>

These codes work in a similar fashion to codes $D8 to $E2 but for words in which the dynamic counter code extends above bit 7. For example, if it is required that bits 0 to 10 of the dynamic tag word contain the dynamic counter code and bits 11 to 15 the source identification code, then the mask should be set to $07.

<u>Codes $E2 and $EE</u>

These codes are special cases. These codes do not implement a step in the dynamic counter code. Instead, they place, in accordance with the mask bits, the two's complement of the last data word transmitted with the flag code $D8 or $E4. For example, if the flag code $D8 (or $E4) and the mask $1F is used at the beginning of a message to transmit the data word XXXX XXXX XXX0 0111 and, at the end of the same message, flag code $E2 (or $EE) is used, then the data word XXXX XXXX XXX1 1001 will be transmitted. The bits shown as X will be determined by the data word associated with the flags.

Codes $E0 and $EC are also special cases similar to $E2 and $EE. The difference is that any overflow from the two's complement is added into the word to be output (i.e., if in the example above, the dynamic counter code had been 00000 and the data word associated with the flag $E0 was $1240, then $1260 would be transmitted).

4.2.9.2 Checksum (Code $F8)

This code instructs the processor to transmit the checksum for the message.

4.2.9.3 Time Stamp (Code $F9)

This code instructs the processor to transmit the current time stamp value.

4.2.9.4 Sawtooth (Codes $FA to $FF)

These codes instruct the processor to transmit an index value that is incremented according to the step register value.

4.2.10 Received (Rx) Words

A number of locations are used to save the data received from the Remote Terminal in response to a command. This data consists of the status word returned by the terminal and the data words, if any. The flag byte, located $10001 above the data word, contains one of the following values to identify the data word. The most significant bit of this byte is set on the last word received.

Flag Code	**Description**
$00	Data Word
$01	Status Word
$02	No Response

4.3 REMOTE TERMINAL OPERATION

The interface, when operating in Remote Terminal mode, is capable of simulating all terminals each with a maximum of 14 sub-addresses or any combination up to this figure, with unique transmit and receive data. When enabled, each terminal is capable of supporting all MIL-STD-1553B transfers. When disabled, the terminal can act as a passive monitor storing all the data from "live" RTs. Each Remote Terminal can be individually enabled and disabled using the flag byte located $10001 above the status word register. Each terminal is enabled by writing a non-zero into the appropriate byte location. This location is also used for the dynamic tag mask. In RT mode, flag codes $D8 to $E2 must be used with the mask set to $FF. Using flag codes $E4 to $EE with mask set to $00 will disable the RT.

The interface is capable of supporting four different responses to mode commands. These responses are:

Flag Code	**Description**
$F0	Status Word only
$F2	Status Word + One Data Word
$F4	Above + Clear SRQ bit
$F6	Update Time Stamp Using Data Word

The interface allows the response type to be selected for all possible mode codes for all terminals individually programmed. Selecting the required response for each mode code is achieved by writing the select code into a location in the mode code map. This map is situated in the byte area of the interface memory and starts at address base + $10001. The address of the required select byte is formed as follows:

OFFSET + 1 0000 0RRR RRMM MMM1

where, RRRRR is the terminal address.
MMMMM is the mode code number.

If the mode code is a receive mode code or is unused, then the select byte must be zero. If the mode code response selected includes an additional data word, then this data word is taken from the word location $10001 below the select byte.

4.3.1 Pointers

The data areas used by each Remote terminal to either transmit data from or store received data into are pointed to by pointers. The pointers are found in the word memory area and consist of two fixed size arrays based on a pointer per RT/SA combination. The address of the required pointer can be formed as follows:

OFFSET + 0 0000 1RRR RRSS SSS0 for the transmit data pointers.

OFFSET + 0 0001 0RRR RRSS SSS0 for the receive data pointers.

where, RRRRR is the terminal address,
SSSSS is the subaddress.

At the byte location $10001 above each pointer location is a guard flag. This flag, if used, can inform the host that the data area pointed to by the associated pointer is currently being accessed and that the integrity of the data may be suspect. The guard flag is non-zero the data area is being accessed.

Note: The value entered in the pointer locations must be scaled for the on-board processor. This is done by dividing the address by two.

4.3.2 Data

The areas for the transmit and receive data must lie in the region bounded by the transmit pointers and the status word registers and must be contiguous. This is the only limitation placed on the use of this area. This means that more than one RT/SA TX or RX pointer may point to single block of memory. This allows unused RT/SA combinations to point to the same transmit or receive data.

The byte locations $10001 above each data word are used to convey further information about the transmit and receive data. For transmit data these flags are used to modify the data transmitted in the same manner as the transmit data in Bus Controller mode. For receive data, the flags are used to indicate the validity of the received message and to mark the end of the received data. This is done using the following codes:

Flag Code	Description
$00	Valid Data Word
$80	End of Message
$81	EOM due to Error

4.4 BUFFERED MULTIPLE REMOTE TERMINAL (BMRT) OPERATION

The BMRT mode is essentially a Multi-Remote Terminal Mode with the interface able to emulate or monitor up to 32 Remote Terminals (RTs). Data to be transmitted by the interface is handled in an identical manner to the MRT mode. Received data, however, is not "mailboxed" on an RT/SA basis as in the MRT mode. Instead, it is put into "circulating ring buffers" of input messages arranged on an RT/SA basis. This allows the interface to maintain multiple copies of the "same" message as defined by the RT/SA combination. This allows the user to handle multiplexed data messages.

4.4.1 Pointers

The transmit data pointers operate as in the MRT mode. The receive data pointers point to "circulating ring buffers" on an RT/SA basis. If the receiver data buffer pointer is zero no data is stored for that RT/SA.

4.4.2 Ring Buffers

Each ring buffer has a fixed buffer header and a user-definable number of buffer entries. Each buffer header is comprised of the following parameters:

IRQ Level/Vector

The IRQ level/status defines the interrupt request level and base interrupt status used when the interface generates a VXI interrupt. This IRQ level/status takes precedence over the common configuration IRQ level/status. If the level is zero then interrupts are disabled. Otherwise, an interrupt is generated each time a command is received for that buffer.

Number of Buffer Entries

The minimum size of each ring buffer is one entry. The maximum number of entries is limited only by available address space.

Ring Buffer Pointer

This is the address of the next entry to be written. It must be initially set by the user, subsequently it is automatically updated. When the ring buffer becomes full (as defined by the "number of buffer entries" in the buffer header), it will "wrap around" to the start of the ring buffer. The value must be scaled for the on-board processor by right shifting the least significant 16 bits of the address by one bit.

Control Word

When the control word is zero, no messages are stored in the buffer. If it is non-zero, the buffer operates normally. Each buffer entry consists of two words, the Command Word (loaded by the interface) and a user defined pointer to the message data. The pointer value must be scaled for the on-board processor by right shifting the least significant 16 bits of the address by one bit. The buffer entries must be continuous with the header. Guard flags operate the same as for the MRT mode.

In RT-RT mode, only the receive command is stored. If an error is detected in a message the message up to the error is stored, but the ring buffer pointer is not updated.

4.5 SELF-TEST OPERATION

When the Built-In-Test is invoked, the interface performs a number of test on key parts of the interface circuitry, including the processor, memory, registers, and encoders. When the tests are completed, the busy bit in the status register is cleared. The result of the BIT can then be found in the result register. If this register is zero, then all the tests have passed and the interface is functioning normally. If the register is non-zero, then one or more of the tests failed. The meaning of each bit is as follows:

Bit	Test Operation (0 = passed, 1 = failed)
0	Lower memory test with $5555 pattern
1	Upper flag memory test with $5555 pattern
2	Lower memory test with $AAAA pattern
3	Upper flag memory test with $AAAA pattern
4	Lower memory test with $0000 pattern
5	Upper flag memory test with $0000 pattern
6	Checksum Test
7	Time Stamp Test
8	Encoder Test

The version and revision of the firmware are also written to the respective registers for access by the host. However, note that after the BIT has been run and a new operation mode is selected and ran, the version and revision registers may no longer be valid.

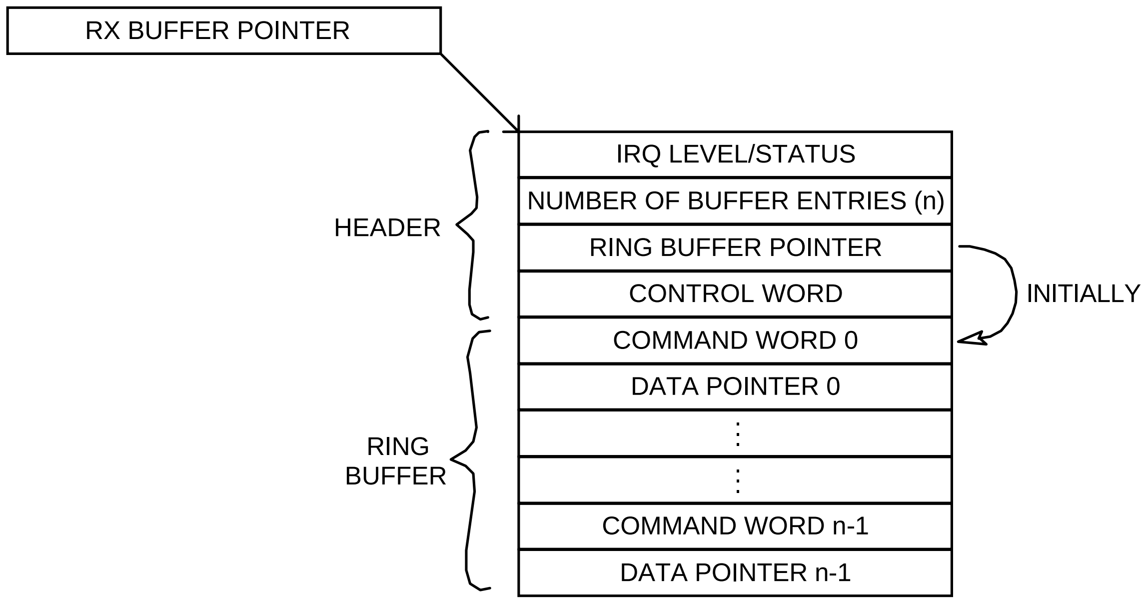


Figure 12. Buffered Multiple Remote Terminal Buffer Format

5.0 MAINTENANCE

5.1 BUILT IN TEST AND DIAGNOSTICS

Refer to 4.5 for self test operations.

5.2 TROUBLE ANALYSIS GUIDE

SYMPTOMS	POSSIBLE CAUSES
Bus time out on A16 Access	1. Logical address incorrectly set. 2. Card incorrectly installed. 3. Faulty card.
Bus time out on A24/A32 Access	1. Offset register incorrectly set. 2. A24/A32 enable bit not set. 3. Card incorrectly installed. 4. Faulty card.
Fails Self Test	1. Faulty card.
Set to run as BC but no output seen on 1553 bus.	1. Incorrectly connected to bus. 2. Root incorrectly set. 3. Amplitude incorrectly set. 4. Bus select incorrectly set. 5. Faulty card.
Ran as BC, then locks up	1. Flag code set to invalid value. 2. Insufficient space allowed for received data. 3. Link pointer incorrectly set. 4. Data pointer incorrectly set. 5. Faulty card.
Set to run as MRT but does not respond on 1553 bus.	1. Incorrectly connected to bus (polarity). 2. Amplitude incorrectly set. 3. RT not enabled. 4. Data pointer incorrectly set. 5. Flag code/mode code set to invalid value. 6. Insufficient space allowed. 7. Faulty card.

APPENDIX A - TIMING SPECIFICATIONS

BUS CONTROLLER MODE.	
Minimum Inter-message Gap	20 µs
REMOTE TERMINAL MODE.	
Minimum Inter-Message Gap	
Simulate	4µs
Broadcast	7µs
Monitor	10µs
Response Time	5µs
BUFFERED MRT MODE.	
Tx Command	
Simulate	8µs
Monitor	15µs
Rx Command	
Simulate	13µs
Monitor	13µs
RT-RT	
Both Simulate	16µs
Rx Simulate/Tx Monitor	14µs
Rx Monitor/Tx Simulate	16µs
Both Monitor	10µs
Broadcast	18µs
Broadcast RT-RT	
Tx Simulate	16µs
Tx Monitor	22µs
Broadcast Mode Code	23µs
Response Time	
RT-RT	≤12µs
All Others	5±1µs

APPENDIX B - CONNECTORS

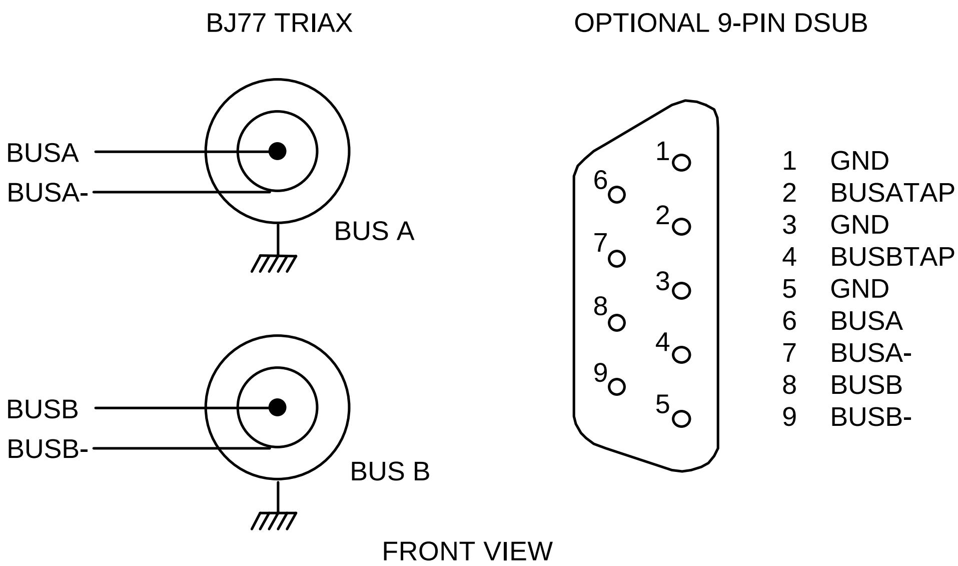
PIN	C	B	A
1	D08	-	D00
2	D09	-	D01
3	D10	-	D02
4	D11	BG0IN*	D03
5	D12	BG0OUT*	D04
6	D13	BG1IN*	D05
7	D14	BG10UT*	D06
8	D15	BG2IN*	D07
9	GND	BG20UT*	GND
10	-	BG3IN*	-
11	-	BG3OUT*	-
12	SYSRESET*	-	DS1*
13	LWORD*	-	DS0*
14	AM5	-	WRITE*
15	A23	-	-
16	A22	AM0	DTACK*
17	A21	AM1	_
18	A20	AM2	_
19	A19	AM3	_
20	A18	GND	IACK*
21	A17	-	IACKIN*
22	A16	-	IACKOUT*
23	A15	GND	AM4
24	A14	IRQ7*	A07
25	A13	IRQ6*	A06
26	A12	IRQ5*	A05
27	A11	IRQ4*	A04
28	A10	IRQ3*	A03
29	A09	IRQ2*	A02
30	A08	IRQ1*	A01
31	+12 V	-	-12 V
32	+5 V	+5 V	+5 V

Figure B-1. P1 Pin Configuration

PIN	C	B	A
1	-	+5V	-
2	-	GND	-
3	GND	-	-
4	-	A24	GND
5	BUSA[1]	A25	BUSA[1]
6	BUSA-[1]	A26	BUSA-[1]
7	GND	A27	-
8	BUSATAP[1]	A28	BUSATAP[1]
9	BUSBTAP[1]	A29	BUSBTAP[1]
10	GND	A30	GND
11	BUSB[1]	A31	BUSB[1]
12	BUSB-[1]	GND	BUSB-[1]
13	-	+5V	-
14	-	-	-
15	-	-	-
16	GND	-	GND
17	-	-	-
18	-	-	-
19	-	-	-
20	-	-	-
21	-	-	-
22	GND	GND	GND
23	-	-	-
24	-	-	-
25	GND	-	+5V
26	-	-	-
27	-	-	-
28	GND	-	GND
29	-	-	-
30	GND	-	MODID
31	-	GND	GND
32	-	+5V	-

[1] Signals only available if jumpers configured to route to P2 local bus. Direct or transformer coupling dependent on jumpers selected. Factory default polarity shown. See 3.2.3 for details.

Figure B-2. P2 Pin Configuration



Note: BUSA and BUSB signals can be either Direct Coupled or Transformer Coupled depending on jumper configurations. Factory default polarity shown.

Figure B-3. Front Panel Connector Configurations

APPENDIX C - BOARD LAYOUT

(insert board layout here)

NOTES:

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