C&H Technologies, Inc. • 445 Round Rock West Drive • Round Rock, TX 78681-5012

(512) 733-2621 • FAX (512) 733-2629 • www.chtech.com

# M228
# 1MSPS Aperture A/D M-Module

The M228 is a 1MSPS 14-bit A/D converter module that samples and selectively stores differential analog signals along with a 32-bit time stamp at a rate up to 1MSPS. The module has the ability to convert and store all data at the specified sample rate or selectively store input values that exceed the range of the programmed aperture window. This technique provides extensive real-time data compression and data extraction for transient type input signals.

In addition, two anti-aliasing filter types, Elliptic and Bessel, plus a bypass provide flexible input conditioning.

## Overview:

**Number of Channels:** 1
**Resolution:** 14-Bit
**Maximum Sample Rate:** 1MSPS
**Input Type:** Bipolar Diff
**Input Impedance:** 10MΩ
**Input Ranges:** ±10V or ±60V
**Gain:** 1 to 1000
**Timestamp:** 32-Bit
**Data Storage:** 32M Samples
**Anti-Aliasing Filter:** Elliptic & Bessel
**Front Panel Inputs/Outputs:** 2/2
**Backplane Triggers** 2

**Operational Features:**

- Programmable Aperture Window with external real-time change capability
- Relative or Absolute Aperture Windowing
- Capture Till Full or Capture Last
- Continuous Time-Stamping while Capture Disabled
- External “Data Stored” signal
- Two Programmable Anti-aliasing Filters (one Bessel response and the other a linear phase elliptic response) plus a bypass mode

**Inputs:**

Each input, front panel and back plane triggers are programmable as the Sample Clock, Conversion Storage Enable, Timestamp Run, Aperture Select, or Force Store signal.

**Outputs:**

Each output, front panel and back plane triggers, are programmable as the Sample Clock (before or after prescaling), Force Store, Aperture Select, A/D Conversion Storage Enable, Timestamp Run, or Value Stored Strobe to allow one M228 to act as the master control for other M228’s.

**I/O Connector:**

44-pin DSUB receptacle

**Power:**

| | |
|---|---|
| +5V | TBDma |
| +12V | TBDma |
| -12V | TBDma |

## M Module Compliance

Complies with ANSI/VITA Std. 12-1996 for single-wide MA Modules

| | |
|---|---|
| Addressing | A8 |
| Data | 32-Bit |
| Interrupts | INTA |
| Triggers | TRIGA/B |

## Temperature:

| | |
|---|---|
| Operating | 0°C to 50°C |
| Storage | -40°C to 70°C |

## Applications

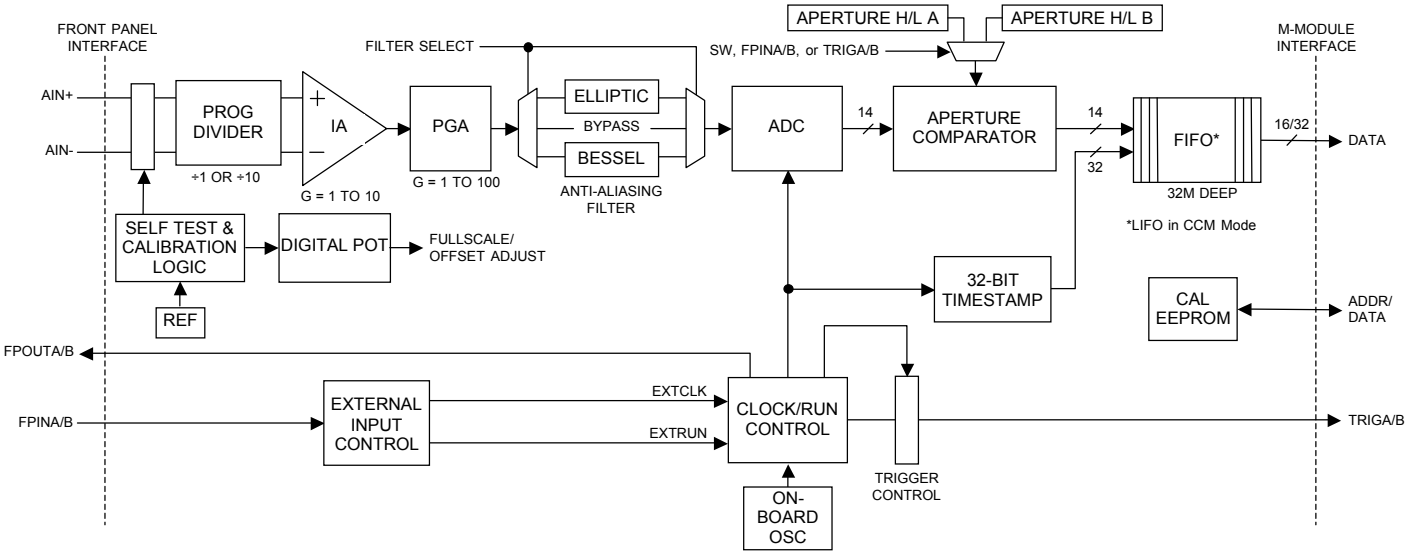
- Acquisition of transient signals
- Real-time data compression
- General A/D Conversion

## Ordering Information

11030500-0001

## Additional Information

User Manuals for C&H carriers and this module can be found on our website at www.chtech.com.




# Specifications:

## A/D Converter:

| | | |
|---|---|---|
| Resolution | | 14 bits |
| Integral Linearity Error | | ±1 LSB |
| Differential Linearity Error | | ±1 LSB |
| Zero Error | | ±15 LSB |
| Throughput (max) | Warp Mode [1] | 1 MSPS |
| | Normal Mode | 800KSPS |
| Zero Offset Error (max) [2] | | TBD mV |
| Full Scale Error [2] | | TBD % + TBD mV |
| Signal to Noise Ratio | | 85.5 dB |

## Signal Input Conditioning:

| | | |
|---|---|---|
| Input Range | normal (G=1) | ±10V |
| | ÷10 active (G=1) | ±60V |
| Common Mode Voltage Range (dc to 50KHz) | | ±13V |
| Common Mode Rejection Ration | | 80dB |
| Input Impedance | differential | 20MΩ |
| | common-mode | 10MΩ |
| | ÷10 active | 10MΩ |
| Divider | programmable | 1 to ÷10 |
| Gain overall | | 1 to 1000 V/V |
| front end | | 1, 2, 5,or 10 V/V |
| back end | | 1, 2, 5, 10, 20, 50,or 100 V/V |
| Filter Cutoff Frequencies | Elliptic | 1.6 - 416 KHz |
| | Bessel | 0.3 - 88 KHz |
| Group Delay | Elliptic, $f_c$=208KHz | 11.7 - 14.1µs |
| | Bessel, $f_c$=88KHz | 6-8µs |
| Passband Ripple [3] | Elliptic, $f_c$=208KHz | TBD |
| | Bessel, $f_c$=88KHz | TBD |
| Filter Roll Off | Elliptic at 1.5 x $f_c$ | 57dB |
| | Elliptic at 6.0 x $f_c$ | 80dB |
| | Bessel at 1.5 x $f_c$ | 5dB |
| | Bessel at 6.0 x $f_c$ | 80dB |

## Input Sample Clock:

| | | |
|---|---|---|
| Accuracy | | ±0.01% |
| Frequency (incremental) [4] | | 10Hz to 1MHz |
| Jitter (max) | | ±500ps |

## Calibration References:

| | | |
|---|---|---|
| Accuracy | ±0.5V | ±0.35% |
| | ±10V | ±0.1% |
| Temperature Coefficient | ±0.5V | 25ppm/°C |
| | ±10V | 50ppm/°C |

## External Inputs (FPINA/B):

| | | |
|---|---|---|
| Input Threshold | programmable | -5.0 to +5.0V |
| Input Impedance | programmable | 50Ω/100KΩ |
| Pulse Width (min) | | 5ns |
| Frequency (max) [5] | | 50MHz |
| Maximum Input Level | no damage, pwr off | ±40V |
| | no damage, pwr on | ±36V |

## External Outputs (FPOUTA/B):

| | | |
|---|---|---|
| Output Level | $V_{OH}$ at -3ma (min) | 2.5V |
| | $V_{OL}$ at 3ma (max) | 0.5V |
| Output Impedance | | 50Ω |

Notes:

1. In Warp Mode, the time between conversions must not exceed 1ms.
2. After calibration
3. Relative to gain at $0.1f_C$.
4. The internal clock rate is 1MHz. A programmable prescaler of 1, 2, 5, 10, 20, 50, 100, and 200 allows various sample rates.
5. This is the maximum frequency that the input logic can accept. The maximum functional frequency is limited by the use of the input signal.