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i3000

M-module Carrier for CompactPCI Bus

User Manual

Version 1.1

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Printed in The Netherlands.

CONTENTS

1. INTRODUCTION

1.1. VALIDITY OF THE MANUAL

This is edition 1.1 of the i3000 user manual and applies to the i3000 M-module Carrier for CompactPCI Bus of revision R0.X, where 0 is the version of the PCB and X is the version of the PLD firmware.

1.2. PURPOSE

This manual serves as an instruction for the operation of the i3000 M-module carrier with PCI interface. The i3000 comes with APIS based software examples, these examples are also discussed in this manual.

The i3000 is based on the PCI9050 PCI bus target interface chip of PLX Technology. For optimal performance the PCI9050 interface chip offers a wide variety of functions, a detailed description of these functions is not part of this manual.

1.3. SCOPE

The scope of this manual is the usage of the i3000 M-module Carrier for CompactPCI Bus.

1.4. DEFINITIONS, ACRONYMS AND ABBREVIATIONS

AcQ	AcQuisition Technology bv
APIS	AcQuisition Platform Interface Software
CompactPCI	PCI with a different physical form factor
DSP	Digital Signal Processor
ESD	Electronic Static Discharge
M-module	Mezzanine I/O concept according to the M-module specification
PCI	Peripheral Component Interconnect
PLD	Programmable Logic Device

1.5. NOTES CONCERNING THE NOMENCLATURE

Hex numbers are marked with a leading “0x”-sign: for example: 0x20 or 0xff.

File names are represented in italic: *filename.txt*.

Code examples are printed in `courier`.

The jumpers are designated by a ‘J’, and a serial number. When specifying wether a jumper should be connected or removed it is referred to solely by this designation if it has only one position (e.g., ‘J5 connected’). However, if the jumper has more than one position, it is also indicated which pins are connected to each other (e.g. ‘J8, 1-2’). Pin 1 of a jumper is always marked in the configuration diagram.

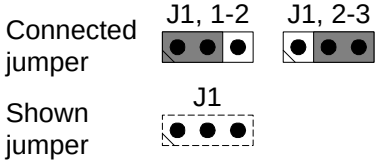

Figure 1 Example jumper nomenclature

In some illustrations jumpers are shown merely for purposes of orientation. In this case they are indicated with a dotted line. Their correct setting is described in another chapter.

Active-low signals are represented by a trailing asterisks (i.e. IACK*).

1.6. OVERVIEW

In chapter 2 a description of the i3000 hardware can be found. Chapter 3 covers the installation and setup of the card as well as mounting M-modules. In chapter 4 the operation and the usage of the i3000 is described The i3000 is distributed with an APIS based demo application which is described in chapter 5. Finally this document contains an annex containing a bibliography, component image, technical data and the document history.

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2. PRODUCT OVERVIEW

2.1. INTRODUCTION

The i3000 provides a bridge between the CompactPCI bus and the M-module interface. The i3000 has a 3U form factor. One M-module can be mounted on the i3000.

The M-module interface of the i3000 complies with the M-module Specification. The M-module specification is ANSI approved. The M-module interface as implemented on the i3000 features A8, A24, D16 and D32 access types.

The PCI interface is PCI Specification 2.1 Compliant, slave only. The PCI to M-module bridge is implemented using the PCI9050 PCI Bus Target Interface Chip of PLX Technology Inc.

2.2. TECHNICAL OVERVIEW

Below an overview of the i3000 is listed.

PCI interface
- PCI Specification 2.1 Compliant Target Interface
- M-module interface runs asynchronously to the PCI clock
- Supports Big/Little Endian Byte Conversion

M-module interface
- 1 M-module Interface (A08/A24, D16/D32)
- INTA software-end-of interrupt supported

Connections
- Via CompactPCI connector to PCI bus
- Access to M-module I/O via 25 pole sub-D connector on the front of the M-module

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3. INSTALLATION AND SETUP

3.1. UNPACKING THE HARDWARE

The hardware is shipped in an ESD protective container. Before unpacking the hardware, make sure that this takes place in an environment with controlled static electricity. The following recommendations should be followed:

- Make sure your body is discharged to the static voltage level on the floor, table and system chassis by wearing a conductive wrist-chain connected to a common reference point.
- If a conductive wrist-chain is not available, touch the surface where the board is to be put (like table, chassis etc.) before unpacking the board.
- Leave the board only on surfaces with controlled static characteristics, i.e. specially designed anti static table covers.
- If handling the board over to another person, touch this persons hand, wrist etc. to discharge any static potential.

IMPORTANT: Never put the hardware on top of the conductive plastic bag in which the hardware is shipped. The external surface of this bag is highly conductive and may cause rapid static discharge causing damage. (The internal surface of the bag is static dissipative.)

Inspect the hardware to verify that no mechanical damage appears to have occurred. Please report any discrepancies or damage to your distributor or to AcQuisition Technology immediately and do not install the hardware.

3.2. JUMPERS

The i3000 contains one jumper: J3. This jumper, when closed, puts the i3000 onboard programmable logic device (PLD) in programming mode which allows the PLD to be programmed via the PCI bus.

For normal operation this jumper must be open. In case of a firmware update, the instructions that come with the update must be followed carefully.

3.3. CompactPCI Interface Connector

The following table provides signal names for the CompactPCI connector J1 as used on the i3000.

Pin	Z	A	B	C	D	E	F
1	GND	+5 V	-12 V	TRST*	+12 V	+5 V	GND
2	GND	TCK	+5 V	TMS	TDO	TDI	GND
3	GND	INTA*	INTB*	INTC*	+5 V	INTD*	GND
4	GND	BRSVP1A4	GND	V(I/O)	INTP	INTS	GND
5	GND	BRSVP1A5	BRSVP1B5	RST*	GND	GNT*	GND
6	GND	REQ*	GND	+3.3 V	CLK	AD[31]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
9	GND	C/BE[3]*	IDSEL	AD[23]	GND	AD[22]	GND
10	GND	AD[21]	GND	+3.3 V	AD[20]	AD[19]	GND
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]*	GND
12-14	Key area						
15	GND	+3.3 V	FRAME*	IRDY*	GND	TRDY*	GND
16	GND	DEVSEL*	GND	V(I/O)	STOP*	LOCK*	GND
17	GND	+3.3 V	SDONE	SBO*	GND	PERR*	GND
18	GND	SERR*	GND	+3.3 V	PAR	C/BE[1]*	GND
19	GND	+3.3 V	AD[15]	AD[14]	GND	AD[13]	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
21	GND	+3.3 V	AD[9]	AD[8]	M66EN	C/BE[0]*	GND
22	GND	AD[7]	GND	+3.3 V	AD[6]	AD[5]	GND
23	GND	+3.3 V	AD[4]	AD[3]	+5 V	AD[2]	GND
24	GND	AD[1]	+5 V	V(I/O)	AD[0]	ACK64*	GND
25	GND	+5 V	REQ64*	ENUM*	+3.3 V	+5 V	GND

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3.4. M-MODULE INTERFACE CONNECTOR

The interface between the i3000 carrier board and an M-module is realized with a 60 pole male header connector J2 (rows A, B and C).

Pin Number	Row A	Row B	Row C
1	CS*	GND	AS*
2	A01	+5V	D16
3	A02	+12V	D17
4	A03	-12V	D18
5	A04	GND	D19
6	A05	DREQ*	D20
7	A06	DACK*	D21
8	A07	GND	D22
9	D08/A16	D00/A08	TRIGA
10	D09/A17	D01/A09	TRIGB
11	D10/A18	D02/A10	D23
12	D11/A19	D03/A11	D24
13	D12/A20	D04/A12	D25
14	D13/A21	D05/A13	D26
15	D14/A22	D06/A14	D27
16	D15/A23	D07/A15	D28
17	DS1*	DS0*	D29
18	DTACK*	WRITE*	D30
19	IACK*	IRQ*	D31
20	RESET*	SYSCLK	DS2*

Orientation of the 60 pole male header connector on the M-module:

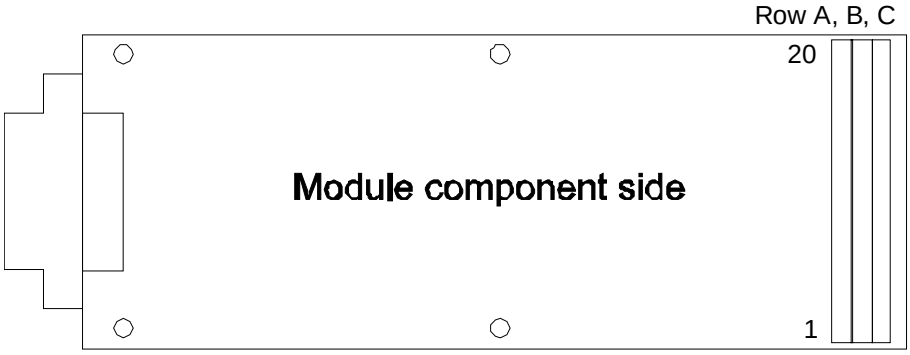

Figure 2 M-module Interface Connector

3.5. MOUNTING AN M-MODULE

One M-module can be fitted on the i3000 carrier board. To plug in a module, position the 2-row 40 pole or 3-row 60-pole M-module interface connector of the module above the 3-row header of the i3000. Then push the module until the 40 or 60-pole header connector is positioned and press the module with care in its place.

Note: With 2-row M-modules row C of the M-module interface connector is left unoccupied.

The module can be secured in its position using four screws (M3 * 5mm), refer to figure 3 for the positions of the mounting screws.

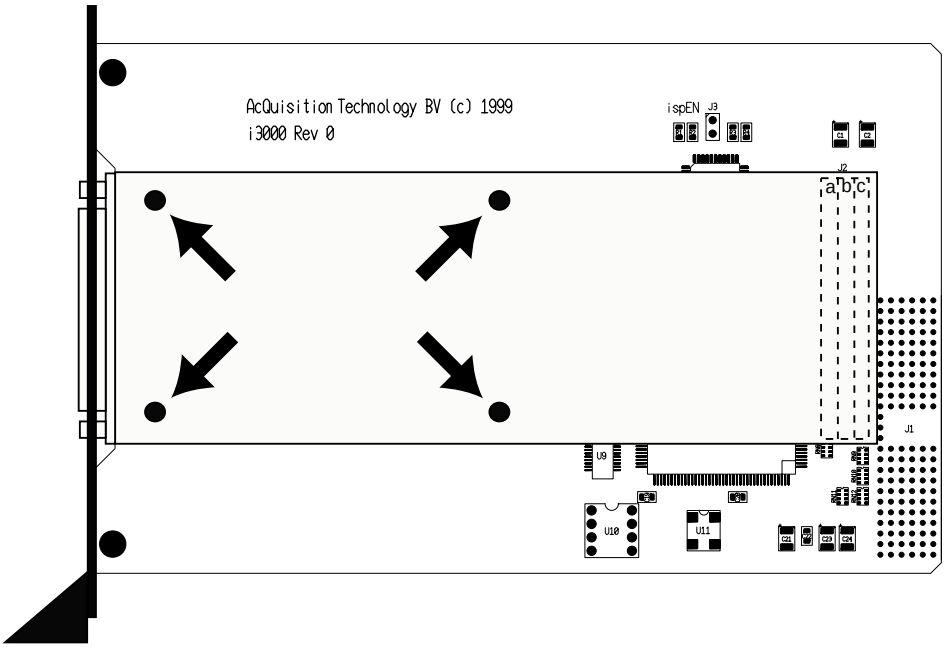

Figure 3 M-module mounting screws

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4. FUNCTIONAL DESCRIPTION

4.1. BLOCK DIAGRAM

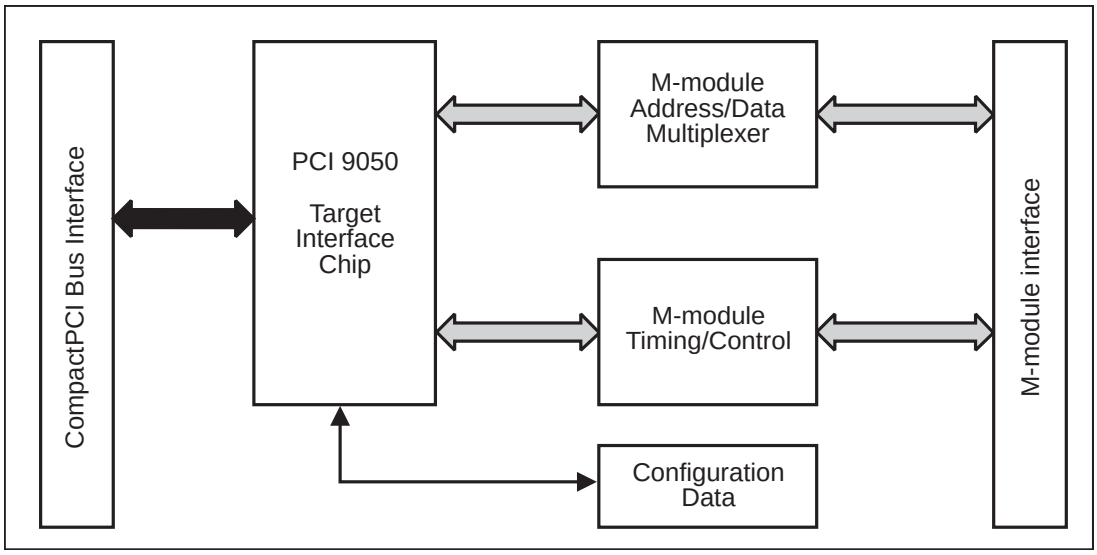

Figure 4 i3000 block diagram

4.2. PCI TO M-MODULE BRIDGE

The PCI to M-module bridge is implemented using the PCI9050 PCI Bus Target Interface Chip by PLX Technology Inc. in combination with a PLD.

The PCI9050 supports both memory mapped and I/O mapped accesses from the PCI bus to the local M-module bus. Bi-directional FIFOs enable high-performance bursting on the local and PCI bus.

The PLD controls the timing of the M-module bus.

4.2.1. LOCAL BUS CONFIGURATION

The i3000 features programmable local bus configuration. The local busses may be either 16 or 32 bit wide and may be multiplexed or non-multiplexed. The PCI9050 also offers big/little endian byte swapping.

The PCI9050 offers four local address spaces. On the i3000 local address space 0 is standard configured for A8/D16 little endian memory mapped M-module accesses and local address space 1 for A8/D16 little endian I/O mapped M-module accesses.

The local bus data lines (LAD0-LAD31) are connected to the M-module data lines (MD0-MD31).
M-module accesses are asynchronous using the READY input of the PCI9050.

Configuration of the PCI interface and local address spaces is done through the PCI9050 configuration registers.

The table below gives an overview of the local memory map:

Local Address	M-module Access Type
0x02000000	A08/D16
0x02000100	A08/D32
0x00000000	A24/D16
0x01000000	A24/D32

The M-module interrupt request line is connected to LINT1 of the PCI9050.
For information on programming and configuration of the PCI9050 please refer to the PCI9050 data sheet.

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4.2.2. CONFIGURATION EEPROM

After reset the PCI9050 reads a serial EEPROM on the card containing factory settings. Default local address space 0 of the PCI 9050 is configured for A08D16 type of M-module accesses mapped in memory space and local address space 1 is configured for A08D16 type of M-module accesses mapped in I/O space.

The table below shows the contents of the serial EEPROM on a standard i3000.

Offset	Contents	Register	Description
00	905010b5	PCIIDR	Device ID, Vendor ID
04	08010001	PCICCR	Class Code
08	300010b5	SYSID	Subsystem ID, Subsystem Vendor ID
0c	00000100	CONF	Max Latency, Min Grant, Int Pin, Int Routing
10	0FFFFF00	LAS0RR	Local Address Space 0 Range
14	0FFFFF01	LAS1RR	Local Address Space 1 Range
18	00000000	LAS2RR	Local Address Space 2 Range
1c	00000000	LAS3RR	Local Address Space 3 Range
20	00000000	EROMRR	Expansion ROM Range
24	02000001	LAS0BA	Local Address Space 0 Base Address (Re-Map)
28	02000001	LAS1BA	Local Address Space 1 Base Address (Re-Map)
2c	00000000	LAS2BA	Local Address Space 2 Base Address (Re-Map)
30	00000000	LAS3BA	Local Address Space 3 Base Address (Re-Map)
34	00000000	EROMBA	Expansion ROM Base Address (Re-Map)
38	00400002	LAS0BRD	Local Address Space 0 Bus Region Descriptors
3c	00400002	LAS1BRD	Local Address Space 1 Bus Region Descriptors
40	00000000	LAS2BRD	Local Address Space 2 Bus Region Descriptors
44	00000000	LAS3BRD	Local Address Space 3 Bus Region Descriptors
48	00000000	EROMBRD	Expansion ROM Bus Region Descriptors
4c	00000000	CS0BASE	Chip Select 0 Base
50	00000000	CS1BASE	Chip Select 1 Base
54	00000000	CS2BASE	Chip Select 2 Base
58	00000000	CS3BASE	Chip Select 3 Base
5c	00000000	INTCSR	Interrupt Control/Status
60	00220000	CNTRL	User I/O, EEPROM, Init Control

WARNING: Reprogramming of the serial EEPROM is strongly discouraged because improper EEPROM contents may cause system boot problems which may require EEPROM replacement.

4.3. M-MODULE INTERFACE

The i3000 provides an M-module interface to a PCI based platform. The wide range of standardized M-modules includes not only process I/O modules but also field buses, DSP and motion control modules as well as special-purpose functions.

The i3000 has the following M-module features:
- 3-row M-modules supported
- 2-row M-modules supported
- A08/A24, D16/D32 address/data range
- INTA supported

4.3.1. STANDARD ACCESSES

The standard M-module interface has an 8-bit address bus. Timing during access is determined solely by the signal SELECT* and DTACK*. This substantially decreases the circuit complexity on the M-modules. On M-modules supporting extended address space, the standard M-module access can be used as an I/O cycle to distinguish between memory type access and register type access.

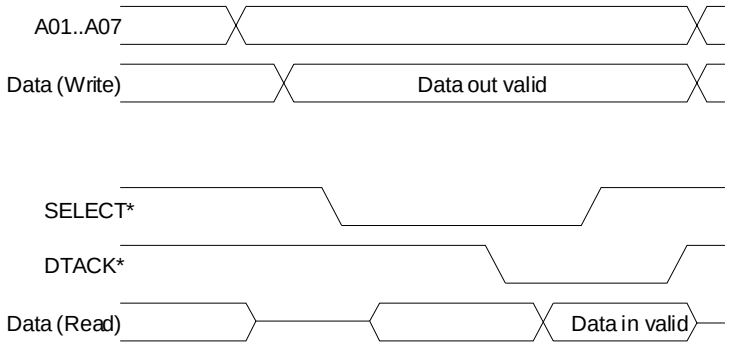

Figure 5 Standard read/write transfer

4.3.2. EXTENDED ACCESSES

The extended address space enables M-modules to be used for applications extending beyond typical I/O functions. The i3000 supports M-modules with an address bus up to 24-bit. The address information is transferred across the data bus in multiplexed mode, reducing the number of pins required. An additional line AS* indicates the current use of the bus. The standard M-module store cycle is embedded in the address transfer cycle.

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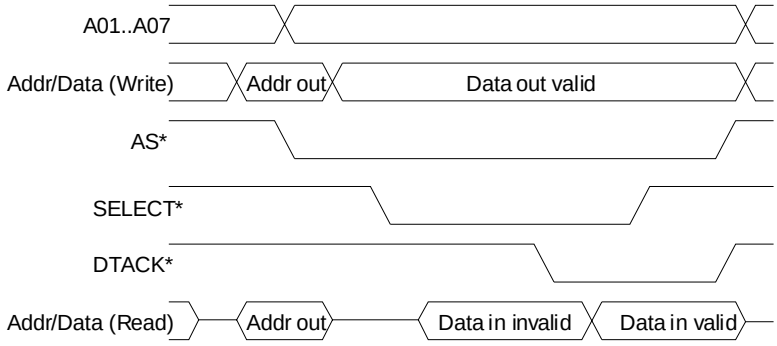

Figure 6 Extended read/write transfers

By mapping both standard and extended M-module access in a different address space as seen from the carrier board, a distinction between a standard and extended M-module access can be made. The table below gives an overview of the local address map in relation to the M-module access type.

Local Address	M-module Access Type
0x02000000	A08/D16
0x02000100	A08/D32
0x00000000	A24/D16
0x01000000	A24/D32

Note: Since the standard M-module access is embedded into the extended M-module access, it is also possible to access a standard M-module in the A24 address range.

4.3.3. BUS TIMER

If an M-module transfer timeout occurs, the i3000 will generate a DTACK*, to prevent the system from lock-out. The transfer timeout is defined as the SELECT* to DTACK* time which is 16 useconds, conforming the M-module Specification.

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5. SOFTWARE SUPPORT

The i3000 comes with an APIS based application that scans the PCI bus for M-modules (modscan). This chapter gives a short description of APIS and the usage of the modscan application.

5.1. APIS

AcQ produces and markets a large number of standard M-modules varying from networking and process I/O to motion control applications. Physically, the M-modules are supported by a large number of hardware platforms: VMEbus, PCI, CompactPCI as well as a wide variety of operating systems: OS-9, Windows NT, Linux etc.

APIS (AcQ's Platform Interface Software) offers a way to program platform independent applications, example- and test software for controlling hardware. Application software written for APIS must only need re-compiling for a particular platform and must be operational with little effort (provided that the application is operating system independent). APIS support for i3000 is currently available for DOS, Windows 95/98/2000/ NT/XP, Linux and Solaris. Please check our website for up-to-date APIS support information. Refer to the APIS Programmer's Manual for more information about APIS.

5.2. MODSCAN

Modscan is an APIS based application that scans the PCI bus for M-modules. The program can be called from the command line and detects all AcQuisition Technology's PCI based M-module carrier boards (i2000, i3000, i3100, etc.). The IDs of the M-modules present on the carrier are displayed. When an M-module does not have an identification EEPROM, ‘Unknown M-module' is displayed. If a slot on a carrier is not occupied with an M-module, it is not displayed in the output.

The display output of modscan may look as follows:

```
M-module scan software by
AcQuisition Technology B.V. 2002

Slot 0: M321
Slot 1: M302
Slot 3: Unknown M-module
Slot 4: M395

Program closed
```

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6. ANNEX

6.1. BIBLIOGRAPHY

M-Module Standard: ANSI/VITA 12-1996, M-Module Specification;
VITA, PO Box 19658, Fountain Hills, AZ 85269, USA
Phone (1)(480)8377486
http://www.vita.com

PCI9050 PCI Bus Target Interface Chip Data sheet
PLX Technology INC, 390 Potrero Ave, Sunnyvale, CA 94086, USA.

PCI Local Bus Specification Revision 2.1
PCI Special Interest Group, 2575 NE Kathryn #17 Hillsboro, OR 97124, USA
Phone (1)(503)6936232, Fax (1)(503)6938344
http://www.pcisig.com

PCI BIOS Specification Revision 2.1
PCI Special Interest Group, 2575 NE Kathryn #17 Hillsboro, OR 97124, USA
Phone (1)(503)6936232, Fax (1)(503)6938344
http://www.pcisig.com

PCI System Architecture, Third Edition
Tom Shanley/Don Anderson
ISBN: 0-201-40993-3

CompactPCI Specification Revision 2.1
PCI Industrial Computer Manufacturers Group, 401 Edgewater Place, Wakefield, MA01880, USA
Phone (1)(781)2469318, Fax (1)(781)2241239
http://www.picmg.com

6.2. COMPONENT IMAGE

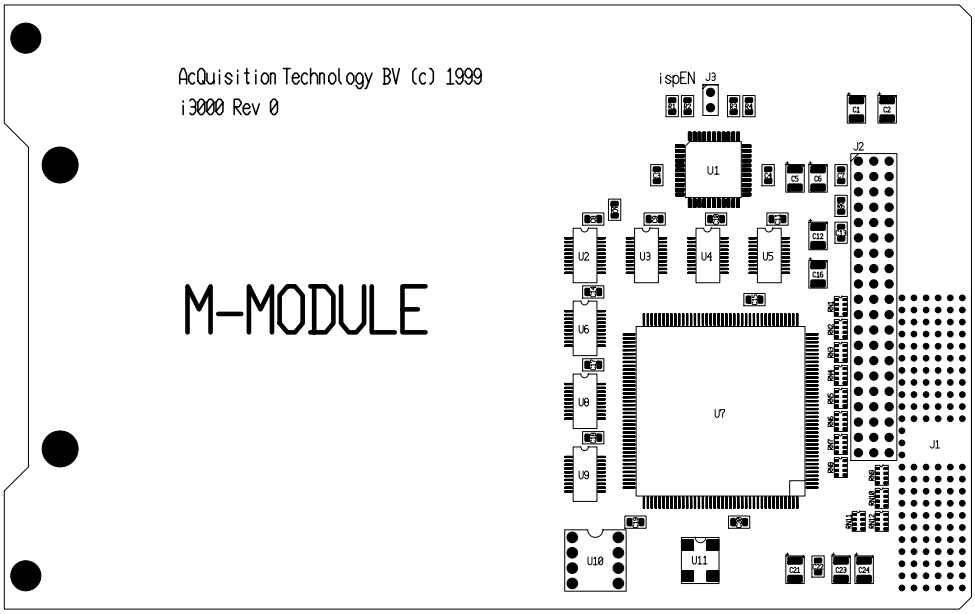

Figure 7 i3000 component view

6.3. TECHNICAL DATA

Slots on the base-board:
Requires one CompactPCI slot.

Connection:
To base-board via CompactPCI connector.
1 x M-module interface.

Power supply:
+5VDC ±10%, typical 400mA (without an M-module mounted).

Temperature range:
Operating: 0..+60EC.
Storage : -20..+70EC.

Humidity:
Class F, non-condensing.

6.4. DOCUMENT HISTORY

- Version 1.0
  First release

- Version 1.1
  New layout
  Software support changed

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