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i3100

Quad M-module Carrier for CompactPCI Bus

User Manual

Version 1.1

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CONTENTS

1. INTRODUCTION

1.1. VALIDITY OF THE MANUAL

This is edition 1.1 of the i3100 user manual and applies to the i3100 CompactPCI M-module carrier board of revision R0.X, where 0 is the version of the PCB and X is the version of the PLD firmware.

1.2. PURPOSE

This manual serves as instruction for the operation of the i3100 M-module carrier board with CompactPCI interface. The i3100 comes with APIS based software examples, these examples are also discussed in this manual.

The i3100 is based on the PCI9050 PCI bus target interface chip of PLX Technology. For optimal performance the PCI9050 interface chip offers a wide variety of functions, a detailed description of these functions is not part of this manual. Refer to the PCI9050 data sheet for more information.

1.3. SCOPE

The scope of this manual is the usage of the i3100 Quad M-module Carrier for CompactPCI.

1.4. DEFINITIONS, ACRONYMS AND ABBREVIATIONS

AcQ	AcQuisition Technology bv
APIS	AcQuisition Platform Interface Software
CompactPCI	PCI with a different physical form factor
DSP	Digital Signal Processor
ESD	Electronic Static Discharge
M-module	Mezzanine I/O concept according to the M-module specification
PCI	Peripheral Component Interconnect

1.5. NOTES CONCERNING THE NOMENCLATURE

Hex numbers are marked with a leading “0x”-sign: for example: 0x20 or 0xff.

File names are represented in italic: *filename.txt*.

Code examples are printed in `courier`.

Active-low signals are represented by a trailing asterisks (i.e. IACK*).

1.6. OVERVIEW

In chapter 2 a description of the i3100 hardware can be found. Chapter 3 covers the installation and setup of the card as well as mounting M-modules. In chapter 4 the operation and the usage of the i3100 is described. The i3100 is distributed with an APIS based demo application which is described in chapter 5. Finally this document contains an annex containing a bibliography, component image, technical data and the document history.

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2. PRODUCT OVERVIEW

2.1. INTRODUCTION

The i3100 provides a high-performance CompactPCI bus gateway to the M-module interface. The i3100 has a 6U form factor. Four M-modules can be mounted on the i3100.

The M-module interface of the i3100 complies with the M-module specification. The M-module specification is ANSI approved. The M-module interface features A8, A24, D16 and D32 access types.

The PCI interface is PCI Specification 2.1 Compliant, slave only. The PCI to M-module bridge is implemented using the PCI9050 PCI Bus Target Interface Chip of PLX Technology Inc.

2.2. TECHNICAL OVERVIEW

Below an overview of the functionality of the i3100 is listed.

PCI interface:
- PCI Specification 2.1 Compliant Target Interface
- Bi-directional FIFO for zero wait-state burst operation
- M-module interface runs asynchronously to the PCI clock
- Supports Big/Little Endian Byte Conversion

M-module interface:
- 4 M-module Interfaces (A08/A24, D16/D32)
- INTA software-end-of interrupt supported

I/O Connections:
- Via 25 pole sub-D connector on the front of the M-module
- Via 24 pole I/O conector on the i3100 (rear I/O)
- Via CompactPCI connector to the PCI bus

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3. INSTALLATION AND SETUP

3.1. UNPACKING THE HARDWARE

The hardware is shipped in an ESD protective container. Before unpacking the hardware, make sure that this takes place in an environment with controlled static electricity. The following recommendations should be followed:

- Make sure your body is discharged to the static voltage level on the floor, table and system chassis by wearing a conductive wrist-chain connected to a common reference point.
- If a conductive wrist-chain is not available, touch the surface where the board is to be put (like table, chassis etc.) before unpacking the board.
- Leave the board only on surfaces with controlled static characteristics, i.e. specially designed anti static table covers.
- If handling the board over to another person, touch this persons hand, wrist etc. to discharge any static potential.

IMPORTANT: Never put the hardware on top of the conductive plastic bag in which the hardware is shipped. The external surface of this bag is highly conductive and may cause rapid static discharge causing damage. (The internal surface of the bag is static dissipative.)

Inspect the hardware to verify that no mechanical damage appears to have occurred. Please report any discrepancies or damage to your distributor or to AcQuisition Technology immediately and do not install the hardware.

3.2. CompactPCI Interface Connector

The following table provides signal names for the CompactPCI connector as used on the i3100.

Pin	Z	A	B	C	D	E	F
1	GND	+5 V	-12 V	TRST*	+12 V	+5 V	GND
2	GND	TCK	+5 V	TMS	TDO	TDI	GND
3	GND	INTA*	INTB*	INTC*	+5 V	INTD*	GND
4	GND	BRSVP1A4	GND	V(I/O)	INTP	INTS	GND
5	GND	BRSVP1A5	BRSVP1B5	RST*	GND	GNT*	GND
6	GND	REQ*	GND	+3.3 V	CLK	AD[31]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
9	GND	C/BE[3]*	IDSEL	AD[23]	GND	AD[22]	GND
10	GND	AD[21]	GND	+3.3 V	AD[20]	AD[19]	GND
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]*	GND
12-14	Key area						
15	GND	+3.3 V	FRAME*	IRDY*	GND	TRDY*	GND
16	GND	DEVSEL*	GND	V(I/O)	STOP*	LOCK*	GND
17	GND	+3.3 V	SDONE	SBO*	GND	PERR*	GND
18	GND	SERR*	GND	+3.3 V	PAR	C/BE[1]*	GND
19	GND	+3.3 V	AD[15]	AD[14]	GND	AD[13]	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
21	GND	+3.3 V	AD[9]	AD[8]	M66EN	C/BE[0]*	GND
22	GND	AD[7]	GND	+3.3 V	AD[6]	AD[5]	GND
23	GND	+3.3 V	AD[4]	AD[3]	+5 V	AD[2]	GND
24	GND	AD[1]	+5 V	V(I/O)	AD[0]	ACK64*	GND
25	GND	+5 V	REQ64*	ENUM*	+3.3 V	+5 V	GND

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3.3. PERIPHERAL CONNECTOR

Peripherals can be connected to M-modules in two ways. On the front side of the module a 25-pole sub-D connector (or mechanically equivalent) can be used to connect cables on the front panel of the i3100. Alternatively, a 24-pole header connector interfaces the I/O signals to the i3100 where they are connected to CompactPCI rear I/O connectors J4/J5. The CompactPCI rear I/O connectors J4/J5 are optional. Refer to section 6.2 for positions of the CompactPCI rear I/O connectors J4/J5.

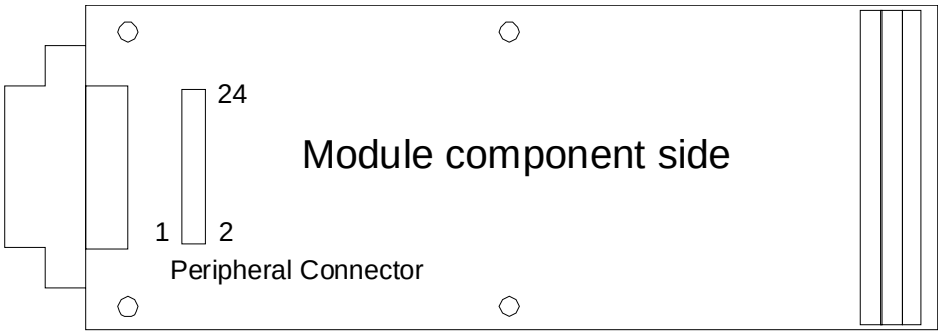

Figure 1

The following tables provide signal names for the CompactPCI rear I/O connectors J4 and J5 as used on the i3100. The signals have the following name Mx-y where x is the M-module and y is the pin number.

Pinout CompactPCI rear I/O connector J4:

Pin	Z	A	B	C	D	E	F
1	GND	reserved	reserved	reserved	reserved	reserved	GND
2	GND	reserved	reserved	reserved	reserved	reserved	GND
3	GND	reserved	reserved	reserved	reserved	reserved	GND
4	GND	reserved	reserved	reserved	reserved	reserved	GND
5	GND	reserved	reserved	reserved	reserved	reserved	GND
6	GND	reserved	reserved	reserved	reserved	reserved	GND
7	GND	reserved	reserved	reserved	reserved	reserved	GND
8	GND	reserved	reserved	reserved	reserved	reserved	GND
9	GND	reserved	reserved	reserved	reserved	reserved	GND
10	GND	reserved	reserved	reserved	reserved	reserved	GND
11	GND	reserved	reserved	reserved	reserved	reserved	GND
12-14	Key area						
15	GND	reserved	reserved	reserved	reserved	reserved	GND
16	GND	reserved	reserved	reserved	reserved	reserved	GND
17	GND	reserved	reserved	reserved	reserved	reserved	GND
18	GND	reserved	reserved	reserved	reserved	reserved	GND
19	GND	reserved	reserved	reserved	reserved	reserved	GND

Pin	Z	A	B	C	D	E	F
20	GND	reserved	reserved	reserved	reserved	reserved	GND
21	GND	reserved	M0-24	M0-23	M0-22	M0-21	GND
22	GND	M0-20	M0-19	M0-18	M0-17	M0-16	GND
23	GND	M0-15	M0-14	M0-13	M0-12	M0-11	GND
24	GND	M0-10	M0-9	M0-8	M0-7	M0-6	GND
25	GND	M0-5	M0-4	M0-3	M0-2	M0-1	GND

Pinout CompactPCI rear I/O connector J5:

Pin	Z	A	B	C	D	E	F
1	GND	reserved	reserved	reserved	reserved	reserved	GND
2	GND	reserved	reserved	reserved	reserved	reserved	GND
3	GND	reserved	M1-24	M1-23	M1-22	M1-21	GND
4	GND	M1-20	M1-19	M1-18	M1-17	M1-16	GND
5	GND	M1-15	M1-14	M1-13	M1-12	M1-11	GND
6	GND	M1-10	M1-9	M1-8	M1-7	M1-6	GND
7	GND	M1-5	M1-4	M1-3	M1-2	M1-1	GND
8	GND	reserved	reserved	reserved	reserved	reserved	GND
9	GND	reserved	reserved	reserved	reserved	reserved	GND
10	GND	reserved	M2-24	M2-23	M2-22	M2-21	GND
11	GND	M2-20	M2-19	M2-18	M2-17	M2-16	GND
12	GND	M2-15	M2-14	M2-13	M2-12	M2-11	GND
13	GND	M2-10	M2-9	M2-8	M2-7	M2-6	GND
14	GND	M2-5	M2-4	M2-3	M2-2	M2-1	GND
15	GND	reserved	reserved	reserved	reserved	reserved	GND
16	GND	reserved	reserved	reserved	reserved	reserved	GND
17	GND	reserved	M3-24	M3-23	M3-22	M3-21	GND
18	GND	M3-20	M3-19	M3-18	M3-17	M3-16	GND
19	GND	M3-15	M3-14	M3-13	M3-12	M3-11	GND
20	GND	M3-10	M3-9	M3-8	M3-7	M3-6	GND
21	GND	M3-5	M3-4	M3-3	M3-2	M3-1	GND
22	GND	reserved	reserved	reserved	reserved	reserved	GND

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3.4. M-MODULE INTERFACE CONNECTOR

The interface between the i3100 carrier board and an M-module is realized with a 60 pole male header connector (rows A, B and C).

Pin Number	Row A	Row B	Row C
1	CS*	GND	AS*
2	A01	+5V	D16
3	A02	+12V	D17
4	A03	-12V	D18
5	A04	GND	D19
6	A05	DREQ*	D20
7	A06	DACK*	D21
8	A07	GND	D22
9	D08/A16	D00/A08	TRIGA
10	D09/A17	D01/A09	TRIGB
11	D10/A18	D02/A10	D23
12	D11/A19	D03/A11	D24
13	D12/A20	D04/A12	D25
14	D13/A21	D05/A13	D26
15	D14/A22	D06/A14	D27
16	D15/A23	D07/A15	D28
17	DS1*	DS0*	D29
18	DTACK*	WRITE*	D30
19	IACK*	IRQ*	D31
20	RESET*	SYSCLK	DS2*

Orientation of the 60 pole male header connector on the M-module:

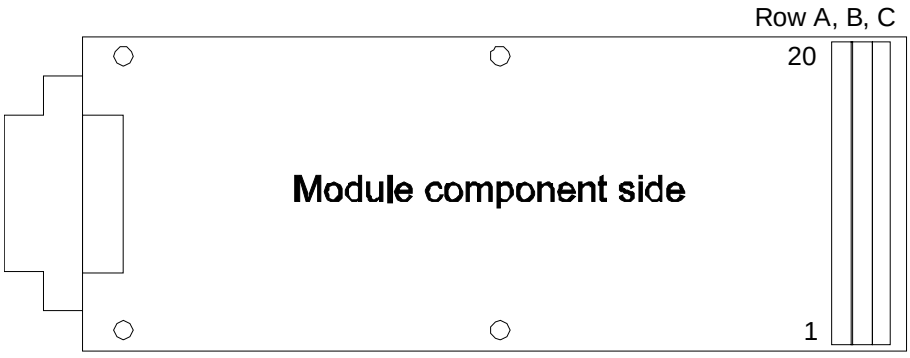

Figure 2 M-module Interface Connector

3.5. MOUNTING AN M-MODULE

Four M-modules can be fitted on the i3100 carrier board. To plug in a module, position the 2-row 40 pole or 3-row 60-pole M-module interface connector of the module above one of the M-module interface connectors of the i3100. Then push the module until the 40 or 60-pole header connector is positioned and press the module with care in its place.

Note: With 2-row M-modules row C of the M-module interface connector is left unoccupied.

The module can be secured in its position using two or four screws (M3 * 5mm), refer to figure 3 for the positions of the mounting screws.

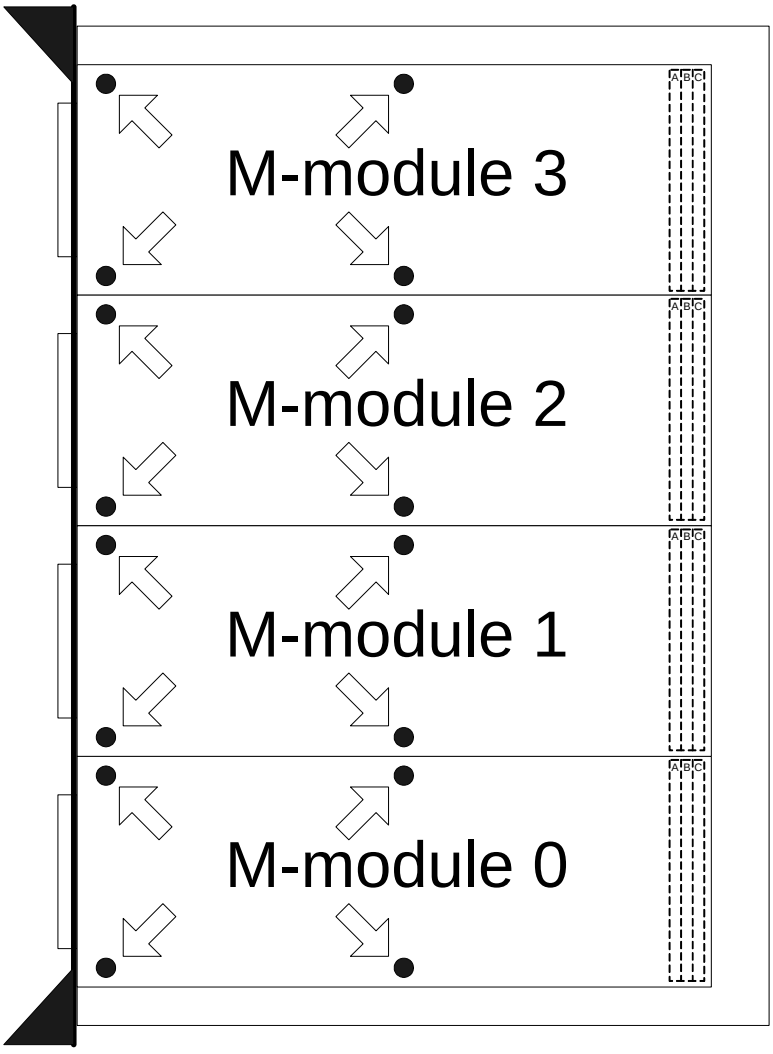

Figure 3 M-module mounting screws

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4. FUNCTIONAL DESCRIPTION

4.1. BLOCK DIAGRAM

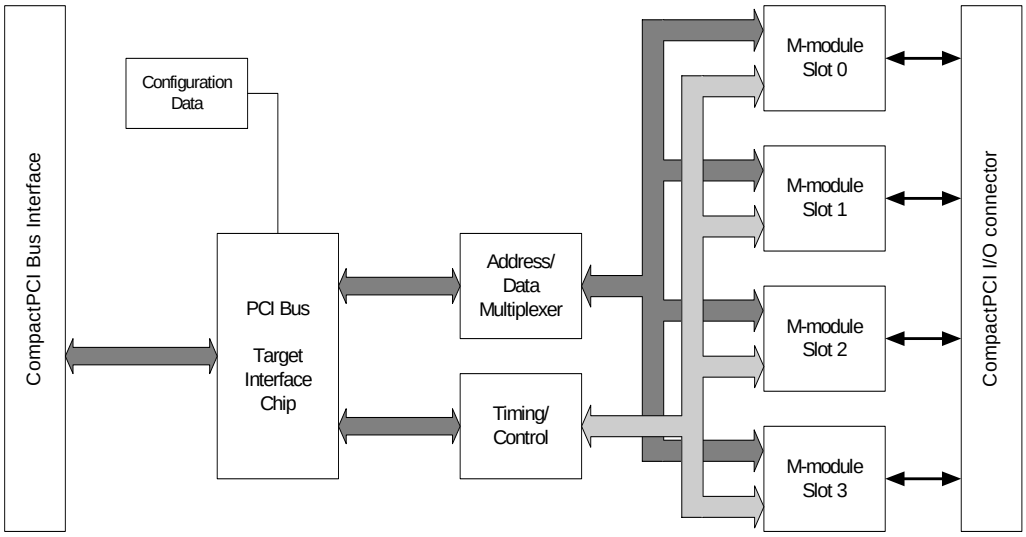

Figure 4 i3100 block diagram

4.2. PCI TO M-MODULE BRIDGE

The PCI to M-module bridge is implemented using the PCI9050 PCI Bus Target Interface Chip by PLX Technology Inc. in combination with a PLD.

The PCI9050 supports both memory mapped and I/O mapped accesses from the PCI bus to the local M-module bus. Bi-directional FIFOs enable high-performance bursting on the local and PCI bus.

The PLD controls the timing of the M-module bus.

4.2.1. LOCAL BUS CONFIGURATION

The i3100 features a programmable local bus configuration which is used by all four M-module slots. The local bus may be either 16 or 32 bit wide and may be multiplexed or non-multiplexed. The PCI9050 also offers big/ little endian byte swapping.

The PCI9050 offers four local address spaces which are not related to the four M-module slots. On the i3100 local address space 0 is configured for A8/D16 little endian memory mapped M-module and control register accesses and local address space 1 for A8/D16 little endian I/O mapped M-module and control register accesses and local address space 2 for A8/D32 little endian memory mapped M-module and control register accesses.

The following table gives an overview of the local address spaces.

Local Address Space	Access Type	Description
0	A08/D16	Memory mapped (little endian)
1	A08/D16	I/O mapped (little endian)
2	A08/D32	Memory mapped (little endian)

The local bus data lines LAD0 to LAD31 are connected to MD0 to MD31 M-module data lines. M-module accesses are asynchronous using the READY input of the PCI9050.

Configuration of the PCI interface and local address spaces is done through the PCI9050 configuration registers.

The table below gives an overview of the valid local addresses:

Local Address Range	Access Type	Description
0x0800 0000-0x0800 00FF	A08/D16	M-module 0
0x0800 0100		Interrupt control register 0
0x0800 0200-0x0800 02FF	A08/D16	M-module 1
0x0800 0300		Interrupt control register 1
0x0800 0400-0x0800 04FF	A08/D16	M-module 2
0x0800 0500		Interrupt control register 2
0x0800 0600-0x0800 06FF	A08/D16	M-module 3
0x0800 0700		Interrupt control register 3
0x0800 0800-0x0800 08FF	A08/D32	M-module 0
0x0800 0900		Interrupt control register 0
0x0800 0A00-0x0800 0AFF	A08/D32	M-module 1
0x0800 0B00		Interrupt control register 1
0x0800 0C00-0x0800 0CFF	A08/D32	M-module 2
0x0800 0D00		Interrupt control register 2
0x0800 0E00-0x0800 0EFF	A08/D32	M-module 3

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Local Address Range	Access Type	Description
0x0800 0F00		Interrupt control register 3
0x0000 0000-0x00FF FFFF	A24/D16	M-module 0
0x0100 0000-0x01FF FFFF	A24/D16	M-module 1
0x0200 0000-0x02FF FFFF	A24/D16	M-module 2
0x0300 0000-0x03FF FFFF	A24/D16	M-module 3
0x0400 0000-0x04FF FFFF	A24/D32	M-module 0
0x0000 0000-0x00FF FFFF	A24/D32	M-module 1
0x0000 0000-0x00FF FFFF	A24/D32	M-module 2
0x0000 0000-0x00FF FFFF	A24/D32	M-module 3

4.2.2. INTERRUPTS

On the i3100 there are three types of interrupts, M-module interrupts, timeout interrupts and address error interrupts. M-module interrupts are connected to LINT1 of the PCI9050, timeout interrupts and address error interrupts are connected to LINT2 of the PCI9050.

Each M-module slot has its own interrupt control register to enable and check the status of the M-module interrupt. Refer to section 4.3.4 for more information about the interrupt control register. For information on programming and configuration of the PCI9050 please refer to the PCI9050 data sheet.

4.2.3. CONFIGURATION EEPROM

After reset the PCI9050 reads a serial eeprom on the card containing factory settings. Default local address space 0 of the PCI 9050 is configured for A08D16 type of M-module accesses mapped in memory space and local address space 1 is configured for A08D16 type of M-module accesses mapped in I/O space.

The following table shows the contents of the serial EEPROM on a standard i3100.

Offset	Contents	Register	Description
00	905010b5	PCIIDR	Device ID, Vendor ID
04	08010001	PCICCR	Class Code
08	310010b5	SYSID	Subsystem ID, Subsystem Vendor ID
0c	00000100	CONF	Max Latency, Min Grant, Int Pin, Int Routing
10	0FFFF800	LAS0RR	Local Address Space 0 Range
14	0FFFF801	LAS1RR	Local Address Space 1 Range
18	0FFFF800	LAS2RR	Local Address Space 2 Range
1c	00000000	LAS3RR	Local Address Space 3 Range
20	00000000	EROMRR	Expansion ROM Range
24	08000001	LAS0BA	Local Address Space 0 Base Address (Re-Map)
28	08000001	LAS1BA	Local Address Space 1 Base Address (Re-Map)
2c	08000801	LAS2BA	Local Address Space 2 Base Address (Re-Map)
30	00000000	LAS3BA	Local Address Space 3 Base Address (Re-Map)
34	00000000	EROMBA	Expansion ROM Base Address (Re-Map)
38	00400002	LAS0BRD	Local Address Space 0 Bus Region Descriptors
3c	00400002	LAS1BRD	Local Address Space 1 Bus Region Descriptors
40	00800002	LAS2BRD	Local Address Space 2 Bus Region Descriptors
44	00000000	LAS3BRD	Local Address Space 3 Bus Region Descriptors
48	00000000	EROMBRD	Expansion ROM Bus Region Descriptors
4c	00000000	CS0BASE	Chip Select 0 Base
50	00000000	CS1BASE	Chip Select 1 Base
54	00000000	CS2BASE	Chip Select 2 Base
58	00000000	CS3BASE	Chip Select 3 Base
5c	00000000	INTCSR	Interrupt Control/Status
60	00220000	CNTRL	User I/O, EEPROM, Init Control

Warning: Reprogramming of the serial EEPROM is strongly discouraged because improper EEPROM contents may cause system boot problems which may require EEPROM replacement.

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4.3. M-MODULE INTERFACE

The i3100 provides an M-module interface to a CompactPCI based platform. The wide range of standardized M-modules includes not only process I/O modules but also interface extensions, field buses, DSP and motion control modules as well as special-purpose functions.

The i3100 has the following M-module features:
- 3 -row M-modules supported
- 2-row M-modules supported
- A08/A24, D16/D32 address/data range
- INTA supported

4.3.1. STANDARD ACCESSES

The standard M-module interface has an 8-bit address bus. Timing during access is determined solely by the signal SELECT* and DTACK*. This substantially decreases the circuit complexity on the M-modules. On M-modules supporting extended address space, the standard M-module access can be used as an I/O cycle to distinguish between memory type access and register type access.

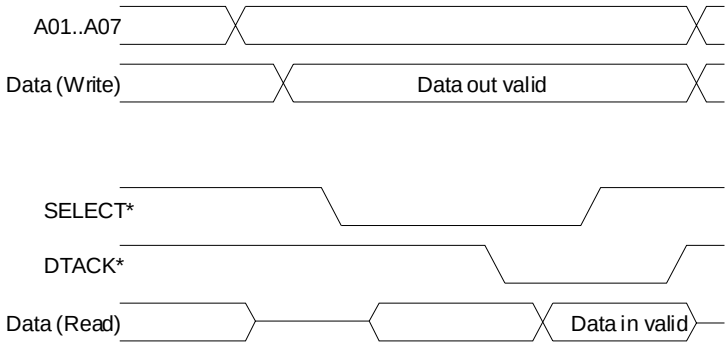

Figure 5 Standard read/write transfer

4.3.2. EXTENDED ACCESSES

The extended address space enables M-modules to be used for applications extending beyond typical I/O functions. The i3100 supports M-modules up to a 24-bit address bus. The address information is transferred across the data bus in multiplexed mode, reducing the number of pins required. An additional line AS* indicates the current use of the bus. The standard M-module store cycle is embedded in the address transfer cycle.

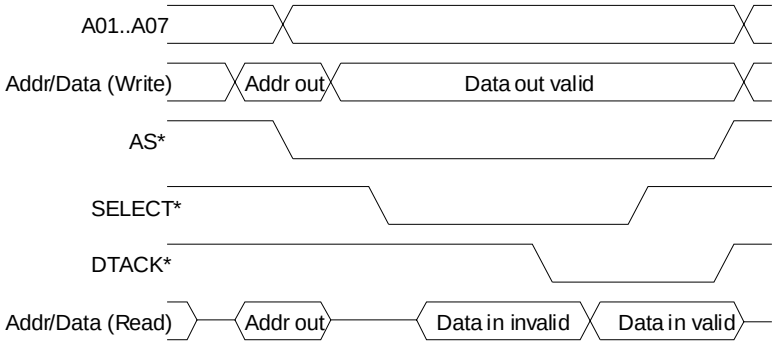

Figure 6 Extended read/write transfers

By mapping both standard and extended M-module access in a different address space as seen from the carrier board, a distinction between a standard and extended M-module access can be made. The table below gives an overview of the local address map in relation to the M-module access type.

Local Address	M-module Access Type
0x08000000	A08/D16
0x08000800	A08/D32
0x00000000	A24/D16
0x04000000	A24/D32

Note: Since the standard M-module access is embedded into the extended M-module access, it is also possible to access a standard M-module in the A24 address range, however since the addresses must be multiplexed, this will result in a slightly slower access.

4.3.3. BUS TIMER

If an M-module transfer timeout occurs, the i3100 will generate a DTACK*, to prevent the system from lock-out.

The transfer timeout is defined as the SELECT* to DTACK* time which is 16 useconds, conforming the M-module Specification.

An interrupt is generated when a transfer timeout occurs, this interrupt is connected to LINT2 of the PCI9050.

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4.3.4. INTERRUPT STATUS CONTROL REGISTER

With the interrupt status control register the interrupts of the i3100 can be controlled. Each M-module slot has its own interrupt status control register and is located at offset 0x100 relative to the local address of the M-module.

IC_REG Offset: 0x100

15	3	2	1	0
not used	AE	TO	IE	IA
Reset:				
	0	0	0	0
Read / Write				

IA Interrupt Active
When asserted, there is an interrupt request from the M-module. The M-module interrupt is connected to LINT1 of the PCI9050.

IE Interrupt Enable
Set this bit to enable M-module interrupts. Clear this bit to disable M-module interrupts.

TO Timeout
When asserted, a transfer timeout has occurred and a timeout interrupt has been generated. Clear pending interrupt by writing a ‘0' to it. The timeout interrupt is connected to LINT2 of the PCI9050.

AE Address Error
When asserted, the PCI bus master has requested single bytes in different words of a double word. This error only occurs in D32 mode and generates an address error interrupt which is connected to LINT2 of the PCI9050. Clear error by writing a ‘0’ to it.

Note: Interrupts must also be enabled on the PCI9050. Refer to PCI9050 data sheet for more information about enabling interrupts.

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5. SOFTWARE SUPPORT

The i3100 comes with an APIS based application that scans the PCI bus for M-modules (modscan). This chapter gives a short description of APIS and the usage of the modscan application.

5.1. APIS

AcQ produces and markets a large number of standard M-modules varying from networking and process I/O to motion control applications. Physically, the M-modules are supported by a large number of hardware platforms: VMEbus, PCI, CompactPCI as well as a wide variety of operating systems: OS-9, Windows NT, Linux etc.

APIS (AcQ's Platform Interface Software) offers a way to program platform independent applications, example- and test software for controlling hardware. Application software written for APIS must only need re-compiling for a particular platform and must be operational with little effort (provided that the application is operating system independent). APIS support for i3100 is currently available for DOS, Windows 95/98/2000/ NT/XP, Linux and Solaris. Please check our website for up-to-date APIS support information. Refer to the APIS Programmer's Manual for more information about APIS.

5.2. MODSCAN

Modscan is an APIS based application that scans the PCI bus for M-modules. The program can be called from the command line and detects all AcQuisition Technology's PCI based M-module carrier boards (i2000, i3000, i3100 etc.). The IDs of the M-modules present on the carrier are displayed. When an M-module does not have an identification EEPROM, ‘Unknown M-module' is displayed. If a slot on a carrier is not occupied with an M-module, it is not displayed in the output.

The display output of modscan may look as follows:

```
M-module scan software by
AcQuisition Technology B.V. 2002

Slot 0: M321
Slot 1: M302
Slot 3: Unknown M-module
Slot 4: M395

Program closed
```

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

6. ANNEX

6.1. BIBLIOGRAPHY

M-Module Standard: ANSI/VITA 12-1996, M-Module Specification;
VITA, PO Box 19658, Fountain Hills, AZ 85269, USA
Phone (1)(480)8377486
http://www.vita.com

PCI9050 PCI Bus Target Interface Chip Data sheet
PLX Technology INC, 390 Potrero Ave, Sunnyvale, CA 94086, USA.

PCI Local Bus Specification Revision 2.1
PCI Special Interest Group, 2575 NE Kathryn #17 Hillsboro, OR 97124, USA
Phone (1)(503)6936232, Fax (1)(503)6938344
http://www.pcisig.com

PCI BIOS Specification Revision 2.1
PCI Special Interest Group, 2575 NE Kathryn #17 Hillsboro, OR 97124, USA
Phone (1)(503)6936232, Fax (1)(503)6938344
http://www.pcisig.com

PCI System Architecture, Third Edition
Tom Shanley/Don Anderson
ISBN: 0-201-40993-3

CompactPCI Specification Revision 2.1
PCI Industrial Computer Manufacturers Group, 401 Edgewater Place, Wakefield, MA01880, USA
Phone (1)(781)2469318, Fax (1)(781)2241239
http://www.picmg.com

6.2. COMPONENT IMAGE

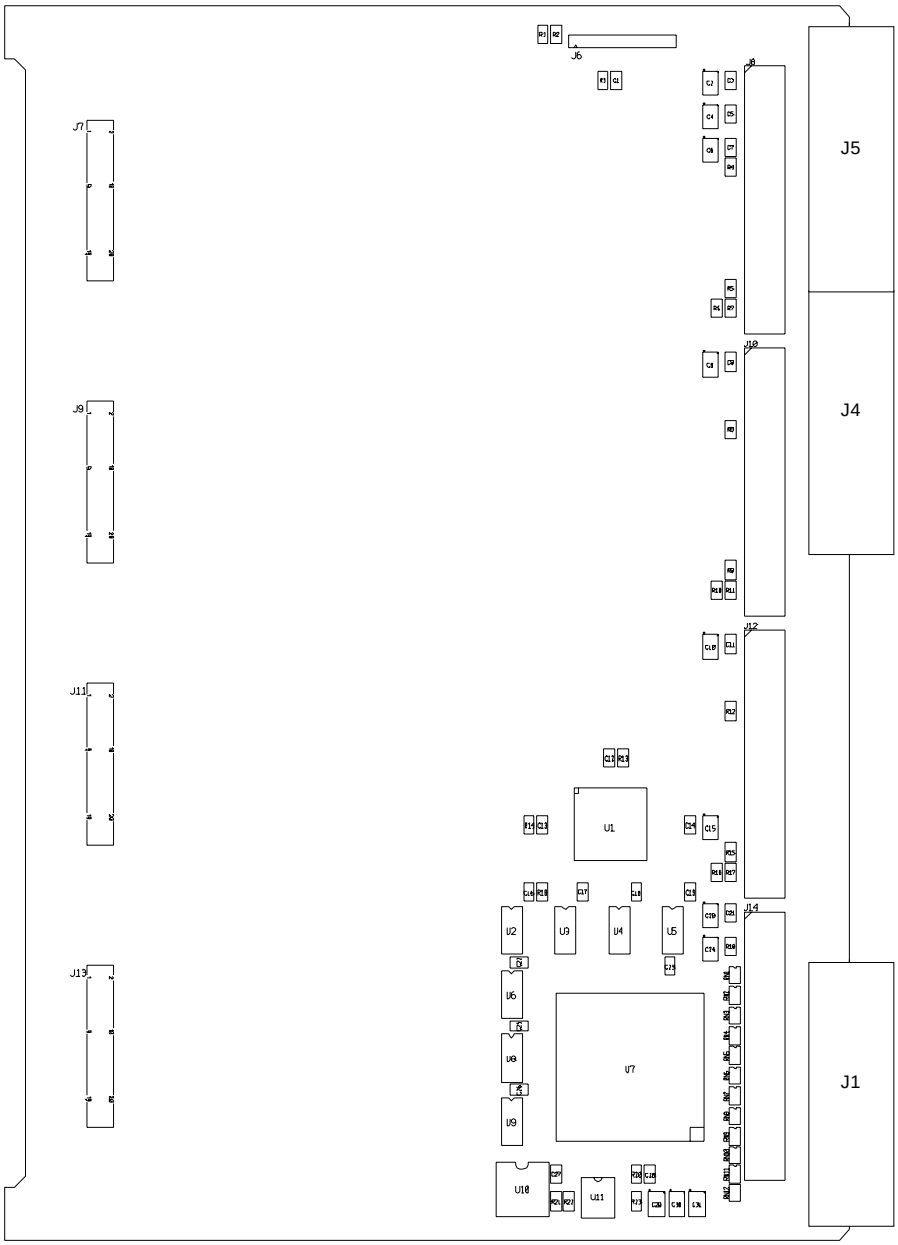

Figure 7 i3100 component view

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6.3. TECHNICAL DATA

Slots on the base-board:
Requires one CompatPCI slot.

Connection:
To base-board via CompactPCI connector.
4x M-module interface.

Power supply:
+5VDC ±10%, typical 400mA (without an M-module mounted)

Temperature range:
Operating: 0..+60 C.
Storage : -20..+70 C.

Humidity:
Class F, non-condensing.

6.4. DOCUMENT HISTORY

- Version 1.0
  First release

- Version 1.1
  New layout
  Mounting an M-module paragraph extended