U S E R ' S M A N U A L

PXI
INDUSTRYPACK
CARRIER

MODEL
PX403S

Manual Part No: 11027304

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INTRODUCTION

This manual describes the operation and use of the C&H Model PX403S PXI IndustryPack® Carrier (Part Number 11027300). This module is one of a number of test and data acquisition/control modules provided by C&H.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction using the higher level interface provided by the driver.

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1.0 GENERAL DESCRIPTION

The PX403S is a single slot 3U form factor PXI/Compact PCI bus compatible carrier module that provides electrical and mechanical support for up to two single wide IndustryPacks (IPs) or one double wide IndustryPack (IP). Each IndustryPack is controlled separately, and appears as an independent device in the PXI/CPCI environment.

1.1 PURPOSE OF EQUIPMENT

This module provides a carrier function for a variety of industry standard plug-in modules that vary in functionality from A/D converters, analog input/output, digital input/output, serial interface, motion control, memory, networking, telecommunication, bus interface, video and many more. With over 350 different modules available in the IndustryPack format, the PX403S is ideal for providing required functions where a PXI or cPCI module does not exist, or for providing more functionality per slot. For a more complete listing of available IPs refer to the following web sites, www.vita.com and www.groupipc.com.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Specifications

- Supports up to two (2) Industry Standard IndustryPacks
- Individual PCI interface for each IP
- Supports usage of PXI bused triggers, STAR triggers, 10MHz system clock
- Special trigger routing and prescaler functionality
- Separate Interrupt Support for each IP
- Isolated +5V, +12V, and -12V supplies each IP
- Supports 8MHz or 32MHz IPs
- 3U form factor
- Up to 100 I/O lines
- 33MHz CPCI compliant
- IP Bus Error Detection
- JTAG boundary scan

1.2.2 Electrical

The module requires the +5V, 3.3V, –12V and +12V power from the PXI back plane. The peak module current (I_{PM}) for the +5 volt supply is 350 milliamps and the +3.3 volt supply is 100 milliamps in addition to any current required by installed IPs. The carrier does not use the +12 and -12 volt supplies.

1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with the PXI bus specification Rev 1.0 for single slot 3U-form factor Modules. The nominal dimensions are 100.0 mm (3.94 in) high x 160 mm (6.3 in) deep. The module is designed for a mainframe with 20.32 mm (0.8 in) spacing between slots. As required by the PXI bus specification, these dimensions are in accordance with those given in the CPCI bus specification (PICMG 2.0 Rev 2.1).

1.2.4 Environmental

The environmental specifications of the module are:

Operating Temperature:	0°C to +55°C
Storage Temperature:	-40°C to +75°C
Humidity:	<95% without condensation

1.2.5 Bus Compliance

The PX403S module complies with the following Specifications.

PCI Bridge Specification:	Revision 1.0
PCI Specification:	Revision 2.1
PXI Specification:	Revision 1.0
CPCI Specification:	PICMG 2.0 R2.1
IP Specification:	ANSI/VITA 4-1995 IP specification Revision 1.0
Manufacturer ID:	$162C_{16}$ (C&H Technologies, Inc.)
Model Code:	$403A_{16}$
PCI Data Transfer:	33MHz/32-bit PCI access
IP Interface:	8 or 32MHz/16-bit
Interrupts:	Full individual interrupt support
Triggers:	Full PXI Trigger Support.

2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

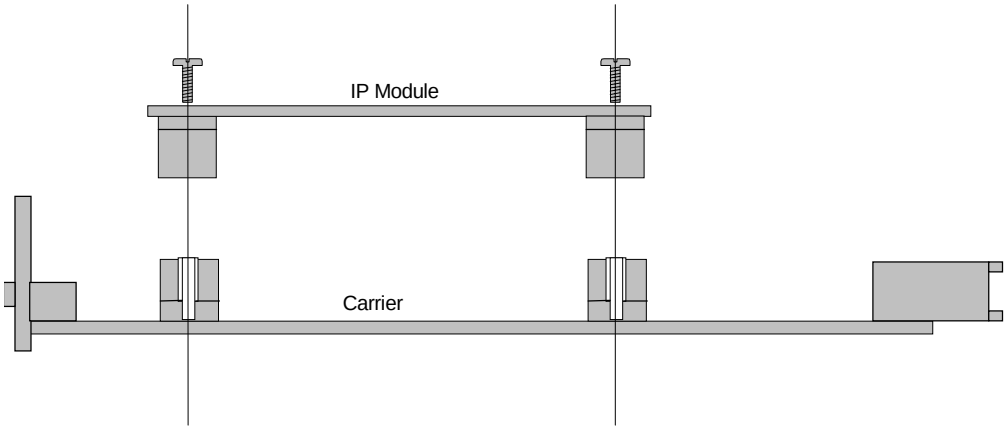
In most cases, the PX403S is individually sealed and packaged for shipment. Verify that there has been no damage to the shipping container. If damage exists then the container should be retained, as it will provide evidence of carrier caused problems. Such problems should be reported to the carrier immediately as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The module contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION OF INDUSTRY PACKS

All IndustryPacks must be installed before the PX403S is installed into the PXI system. IndustryPacks are installed by firmly pressing the two connectors on the IP together with the connectors on the carrier. The connectors are keyed to insure the IP can only be installed correctly. Follow the mounting instructions provided with the IP. The IP manufacturer should have provided mounting hardware.



There are two possible mounting locations on the carrier: A and B. IndustryPacks may be installed into either location. Enable the IP position and memory by following the hardware configuration instructions in Section 4.2.1 Hardware Configuration.

2.3 INSTALLATION OF CARRIER

> **CAUTION: Read the entire User's Manual before proceeding with the installation and application of power.**

Insert the module into the desired PXI or CPCI slot. Apply power. If no obvious problems exist, proceed to communicate with the module as outlined in Section 4.0 OPERATING INSTRUCTIONS.

2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti static bag. Heat-seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum. The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage.

3.0 FUNCTIONAL DESCRIPTION

3.1 GENERAL

The PX403S provides a mechanical and electrical interface for up to two standard Industry Pack modules (or one doublewide module). The carrier provides access to the IndustryPack's ID PROM, I/O Space, and Memory Space(if present). To ease software integration of the individual functions provided by IP modules, the PX403S treats each IP module as an independent device. The PCI-to-PCI bridge technology implemented on the PX403S allows each IP to have individual PCI configuration registers. This allows software applications and drivers to access individual IP functions as truly independent devices. Each IndustryPack is controlled separately, and appears as an independent device in the PXI environment. A simplified functional block diagram of the module is shown in Figure 1.

The PX403S can support Type I, II, and III IP modules. Type I modules have no components on the back of the module. Type II modules have components on the back, but are subject to height restrictions. Type III module have components on the back, without height restrictions. If a Type III module is used, be sure that the IP doesn't violate the slot to slot spacing defined by the PXI or the CPCI specifications. If the IP violates the specification, population of the adjacent slot will not be possible.

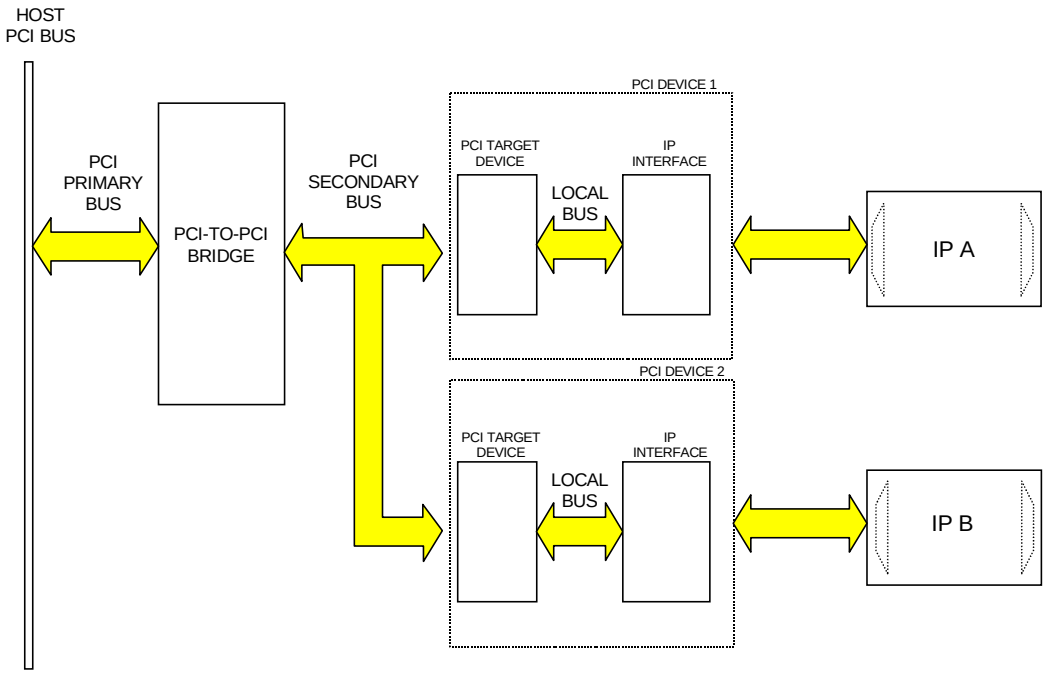


Figure 1. Functional Block Diagram

3.2 INTERFACES

The two IP positions interface electrically and mechanically with industry standard IndustryPack modules meeting the IndustryPack Logic Interface Specification ANSI/VITA 4-1995. The IPs interface to the PX403S through one 50-pin connector mounted to the carrier board. The IP's I/O signals interface through the other 50-pin connector and are routed the front panel connector of the PX403S.

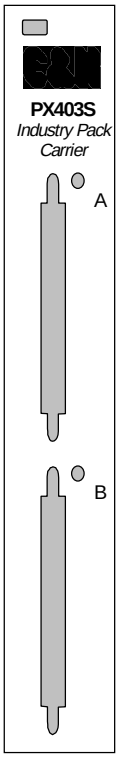


Figure 2. Front Panel

3.3 INDICATORS

The appropriate LED indicator on the front panel illuminates whenever the host processor properly accesses the IP.

3.4 CONNECTORS

3.4.1 Front Panel Connector

The IP's 50 I/O pins are routed through the carrier board to a 50-pin (.8mm) shielded AMP Champ type connector accessible at the front panel of the PX403S. See Appendix A for pin-out details.

Board Connector
AMP part number: 787096-1

Mating Cable Connector
Amp part number: 787131-1

3.4.2 Rear Connectors

The P1 and P2 connectors are configured in accordance with the PXI / CPCI specification. (See Appendix A)

4.0 OPERATING INSTRUCTIONS

4.1 GENERAL

The PX403S is easily configured using a few physical switches and a variety of software registers. The switches allow access to an IP to be individually enabled or disable and allow memory to be allocated or not allocate for an IP, see Figure 3. The software registers provide individual configuration of interrupts, triggers, clock speed, and bus time out for each IP.

4.2 CONFIGURATION

4.2.1 Hardware Configuration

NOTE: Hardware configuration must be done while power to the module is OFF.

IP Modules Enable There is an enable switch for each IP slot. Each switch represents an IP and must be enabled before the carrier will recognize a module as present. When the switch is in the ON position the slot is disabled. Conversely, the IP is enabled when the switch is OFF position.

IP Memory Enable There is a memory enable switch for each IP slot. Each IP Memory Enable switch must be enabled before the carrier will recognize that the module present requires memory. When the switch is in the ON position the slot is assigned memory. Conversely, the IP is not assigned memory when the switch is OFF position.

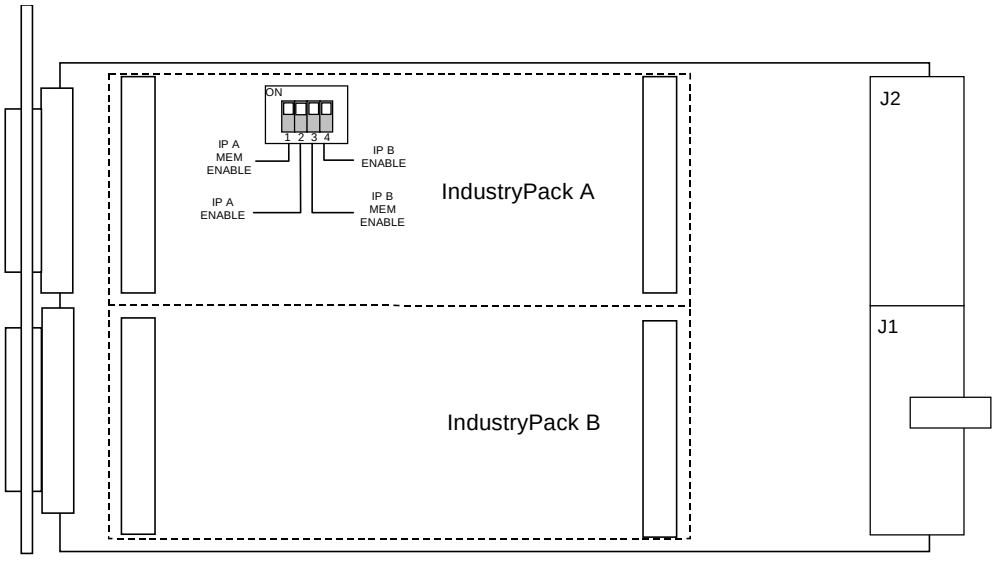


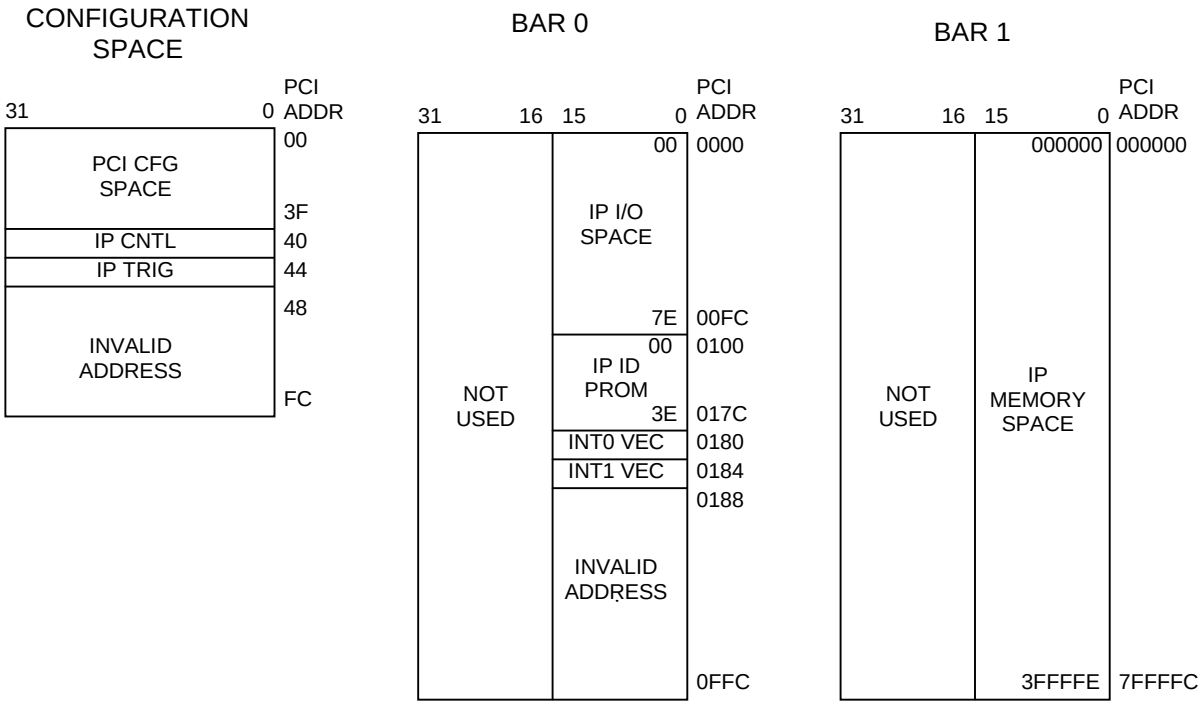
Figure 3. Hardware Configuration

4.2.2 Software Configuration

Each IP enabled on the PX403S has its own PCI Device Number and they appear as device's 1 and 2 on a subordinate PCI bus. The PX403S uses the PCI Configuration, Base Address Register 0 (BAR0) and Base Address Register 1 (BAR1) Space out of the available PCI resources.

The PX403S supports both D16 and D8 (Even/Odd) data access to the IPs. Each IP has its own PCI interface, which means that each IP is independently configured and accessed. The IP resources (ID, I/O, and Memory) are all mapped into PCI memory space. The memory space is fully decoded. If an invalid address is attempted, the PX403S will issue a target abort. The memory map is identical for each IP as indicated in Figure 4. PCI I/O space is not used.

NOTE: Since IPs use 16-bit addressing and PCI use 32-bit addressing, multiply the IP address by two for the correct PCI address.



Note: The PCI address is two times the IP address. The upper 16-bits of a 32-bit PCI read are returned as zeros. Only the lower 16-bits are used on a 32-bit PCI write.

Figure 4. IP Address Map

The PCI and interface control registers are located in the PCI device configuration space. The PCI configuration space is used to control and report information concerning the PCI interface. Most of the registers in the configuration space are used and/or set by the system BIOS. See Appendix B for reference information on these PCI configuration registers.

Several registers within the PCI configuration space are of particular interest. They are the Base Address Registers (BAR0 and BAR1) and PCI user-defined registers (IP CNTL and IP INT). All other software control of an IP is IP dependent and is described in the IP's user manual.

Base Address Registers (BAR0 and BAR1) (Base + 10_{16} and Base + 14_{16}) BAR0 is the base address for the IP I/O Space, ID PROM, and IP interrupt vector registers. The PX403S automatically requests 4Kbytes of PCI memory space and the BIOS should allocate that amount for this address area. BAR1 is the base address for the IP Memory Space. If the IP Memory Enable switch is ON (see 4.2.1), then the PX403S will request 16Mbytes of PCI memory space and the BIOS should allocate that amount for this address area.

IP Interface Status/Control Register (IP CNTL) (Base + 40_{16}) This read/write register is used to control and status interface functions such as reset, clock speed, interrupts, triggers and bus timeout. See Figure 5 for details.

IP Interface Trigger Control Register (IP INT) (Base + 44_{16}) This read/write register is used to configure the PXI Trigger/IP strobe operation. See Figure 6 for details.

IP Status/Control

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	CLR	—	ID	—	—	Time Out (0-7)			—	—	—	CLK	—	—	—	RST
Read	INT	—	ID	—	—	Time Out (0-7)			—	—	—	CLK	IRQ1	IRQ0	ERR	RST

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Write	Reserved															
Read																

CLR ⇨ Clear PCI Interrupt Request (1 = clear PCI Interrupt Pending)
INT ⇨ PCI Interrupt Request (1 = interrupt pending)
ID ⇨ IP ID Write Enable (1 = write enabled (if IP allows writes to ID PROM))
Time Out ⇨ Bus Time Out

00h	3.2 µs
01h	32 µs
02h	320 µs
03h	3.2 ms
04h	32 ms
05h	320 ms
06h	3.2 sec
07h - FFh	Reserved

CLK ⇨ IP Clock Control (0= 8 MHz, 1 = 32 MHz)
IRQ0 ⇨ IP Interrupt Request 0 (1 = pending)
IRQ1 ⇨ IP Interrupt Request 1 (1 = pending)
ERR ⇨ IP Error Indicator (0 = OK, 1 = failure, directly reflects the IP Module Error signal)
RST ⇨ IP Reset (1 = reset IP, leave for >100µs then clear to 0)

Figure 5. IP Status/Control Register

IP Trigger Control

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Trig En (0 – 7)								Prescaler			SEL		DIR	INV	EN
Read	Trig En (0 – 7)								Prescaler			SEL		DIR	INV	EN

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Write	Trig Dir (0 – 7)								Trig Inv (0 – 7)							
Read	Trig Dir (0 – 7)								Trig Inv (0 – 7)							

Trig En (0-7) ⇨ Trigger Bus Enable (1 = enable trigger line, all enabled input triggers are logically OR'ed, default = 0)

Prescaler ⇨ Prescaler Select (Selected clock is divided by this prescaler)

0 0 0	Prescaler = 1 (default)
0 0 1	Prescaler = 2
0 1 0	Prescaler = 5
0 1 1	Prescaler = 10
1 0 0	Prescaler = 20
1 0 1	Prescaler = 50
1 1 0	Prescaler = 100
1 1 1	Prescaler = 200

SEL ⇨ Trigger Select

0 0	None	(default)
0 1	Bussed Triggers	In/Out
1 0	Star Triggers	In only
1 1	10 MHz	In only

DIR ⇨ Strobe Direction (0 = strobe input to IP, 1 = strobe output from IP, default = 0)

INV ⇨ Strobe Invert (1 = inverted, default = 0)

EN ⇨ Strobe Enable (1 = trigger enabled, default = 0)

Trig Dir (0-7) ⇨ Trigger Bus Direction (0 = trigger input to PX403S, 1 = trigger output from PX403S)

Trig Inv (0-7) ⇨ Trigger Bus Invert (1 = Inverted, default = 0)

Figure 6. IP Trigger Control Register

4.3 IP I/O OPERATIONS

The IP's I/O Space and ID PROM areas are accessed as an offset from BAR0. If the IP has on-board memory and the IP memory enable switch is ON, then the IP memory is accessed as an offset from BAR1.

During write transactions, the PX403S issues an auto acknowledge and completes the PCI cycle before the IP issues an acknowledge. For this reason, it is not possible to detect real-time IP write transaction errors. The PX403S does; however, have a timeout timer that prevents the interface from getting into a "hung" state. The PX403S also prevents missing bus transactions, by forcing the host to issue retries until the IP is ready for another transaction. The write cycle time is dependent on the speed of the IP and the number of wait states that are inserted.

During read transactions, the PX403S issues retries until the IP returns a data acknowledge. It then issues a "disconnect with data". If the IP does not acknowledge the cycle, the bus timeout timer will expire and a "target abort" will be issued. The data access cycle time is dependent on the speed of the IP and the number of wait states inserted.

The bus timeout timer is programmable and has several time options available to suit the transaction time required by the IP. The purpose of the timeout timer is to keep the interface from getting into a "hung" state when the IP does not issue an acknowledge. The timer can be programmed to expire from selected times ranging from 3.2 us to 3.2 s.

4.3.1 ID PROM Access

The IP ID PROM data (00_{16} to $3E_{16}$) is mapped to PCI address apace BAR0+100_{16} to BAR0+$17F_{16}$. The format of ID PROM data can be either Type I or Type II. Consult the IP's documentation for details. If the format is Type I, only the lower (odd) byte is valid. The high byte is always FF_{16}.

Table I. ID PROM Contents (Format I)

PCI Address, hex	Register Description
BAR0 + 100	ASCII “I”
BAR0 + 104	ASCII “P”
BAR0 + 108	ASCII “A”
BAR0 + 10C	ASCII “C” or "H"
BAR0 + 110	Manufacturer ID
BAR0 + 114	Model Number
BAR0 + 118	Revision Level
BAR0 + 11C	Reserved
BAR0 + 120	Low Byte Driver ID (Firmware Rev)
BAR0 + 124	High Byte Driver ID
BAR0 + 12C	Number of Bytes Used
BAR0 + 130	CRC
BAR0 + 134 to 17C	IP Module Specific & User Space

4.3.2 I/O Space Access

The IP I/O Space (00_{16} to $7E_{16}$) is mapped to PCI address space BAR0+00_{16} to BAR0+FC_{16}. Since IPs use 16-bit addressing and PCI use 32-bit addressing, the IP address must be multiplied by two for the correct PCI address. When doing 32-bit PCI accesses, only the lower 16-bits are used.

4.3.3 Memory Access

If the installed IP supports on-board memory and IP memory is enabled on the PX403S, the IP Memory Space (000000_{16} to $3FFFFE_{16}$) is mapped to PCI address space BAR1+000000_{16} to BAR0+$7FFFFC_{16}$. Since IPs use 16-bit addressing and PCI use 32-bit addressing, the IP address must be multiplied by two for the correct PCI address. When doing 32-bit PCI accesses, only the lower 16-bits are used.

4.2.4 Interrupts

Each IP can support up to two interrupt requests as specified in the IndustryPack Logic Interface Specification. The interrupt scheme for each PCI interface follows the interrupt binding as recommended by the PCI and CPCI bus specifications. It is up to the Interrupt Service Routine (ISR) to determine the priority of multiple interrupts.

When an IP request an interrupt, a PCI interrupt is requested from the host. The PCI interrupt is cleared by removing the interrupt request from the IP or by writing a 1 to Bit 15 of the IP Status/Control Register (IP CNTL) in the PCI Configuration Space (40_{16}). See Figure 5 for details. Writing to the IP CNTL Register clears the PCI interrupt, but not the IP interrupt. The ISR must handle the IP interrupt according to the IP's documentation.

Since PCI does not use interrupt vectors, the IP interrupt vectors (INT0VEC and INT1VEC) may be read at BAR0+180_{16} and BAR0+184_{16}, respectively, when and only when, the appropriate interrupt request from the IP is pending. If the register is read when an interrupt is not pending, a "target abort" is issued and the value read is $FFFF_{16}$.

4.2.5 Triggers

NOTE: Trigger signals are only supported in PXI systems or custom configured CPCI systems.

The PX403S supports PXI bus triggers, the STAR Trigger line and the 10 MHz system reference clock. The trigger logic is configured using the IP Trigger Control Register in the PCI Configuration Space (44_{16}). See Figure 6 for details.

The trigger logic also provides logical OR'ing and prescaler operations. All enabled PXI input triggers are logically OR'ed before the signal goes to the prescaler. All enabled output triggers reflect the same

output Strobe signal. The prescaler works for both input and output Strobes. The direction is determined by the Strobe Direction control bit. See Figure 7 for details.

The PX403S uses active driver logic (not open-collector) to output the PXI trigger signal to the backplane. Care must be taken to insure that multiple devices are not driving the same trigger line at the same time.

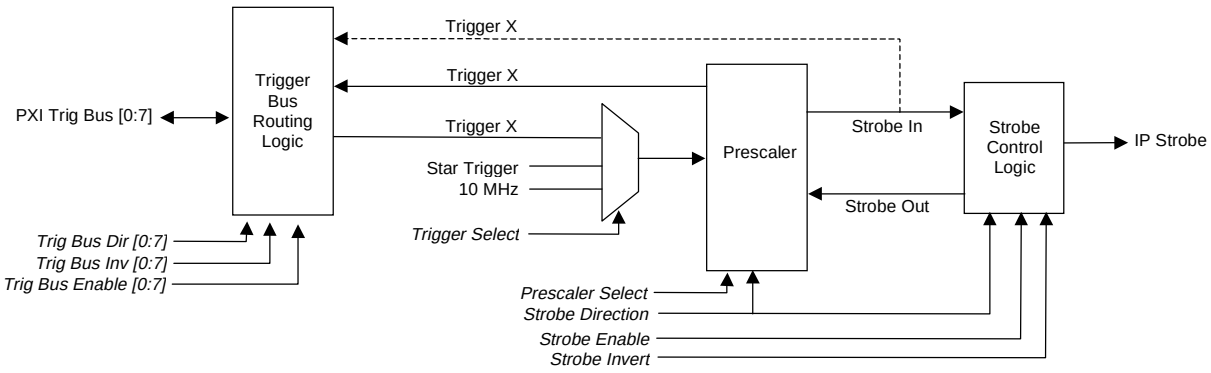
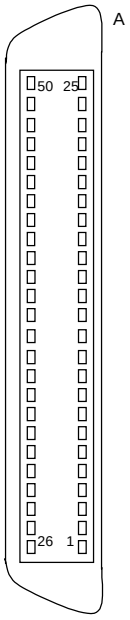
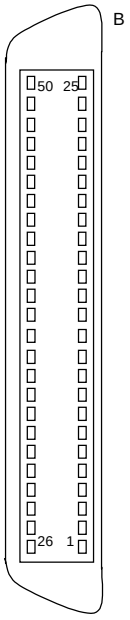


Figure 7. Trigger Functional Diagram

APPENDIX A - CONNECTORS



IP A	
I/O 50	I/O 25
I/O 49	I/O 24
I/O 48	I/O 23
I/O 47	I/O 22
I/O 46	I/O 21
I/O 45	I/O 20
I/O 44	I/O 19
I/O 43	I/O 18
I/O 42	I/O 17
I/O 41	I/O 16
I/O 40	I/O 15
I/O 39	I/O 14
I/O 38	I/O 13
I/O 37	I/O 12
I/O 36	I/O 11
I/O 35	I/O 10
I/O 34	I/O 9
I/O 33	I/O 8
I/O 32	I/O 7
I/O 31	I/O 6
I/O 30	I/O 5
I/O 29	I/O 4
I/O 28	I/O 3
I/O 27	I/O 2
I/O 26	I/O 1



IP B	
I/O 50	I/O 25
I/O 49	I/O 24
I/O 48	I/O 23
I/O 47	I/O 22
I/O 46	I/O 21
I/O 45	I/O 20
I/O 44	I/O 19
I/O 43	I/O 18
I/O 42	I/O 17
I/O 41	I/O 16
I/O 40	I/O 15
I/O 39	I/O 14
I/O 38	I/O 13
I/O 37	I/O 12
I/O 36	I/O 11
I/O 35	I/O 10
I/O 34	I/O 9
I/O 33	I/O 8
I/O 32	I/O 7
I/O 31	I/O 6
I/O 30	I/O 5
I/O 29	I/O 4
I/O 28	I/O 3
I/O 27	I/O 2
I/O 26	I/O 1

(As viewed towards front panel)

Front Panel I/O Connector Pin Configuration

I/O Pin	Signal
1	GND
2	CLK
3	RESET-
4	D0
5	D1
6	D2
7	D3
8	D4
9	D5
10	D6
11	D7
12	D8
13	D9
14	D10
15	D11
16	D12
17	D13
18	D14
19	D15
20	BS0-
21	BS1-
22	-12V
23	+12V
24	+5V
25	GND

I/O Pin	Signal
26	GND
27	+5V
28	R/W-
29	IDSEL-
30	DMAREQ0-
31	MEMSEL-
32	DMAREQ1-
33	INTSEL-
34	DMACK0-
35	IOSEL-
36	reserved
37	A1
38	DMAEND-
39	A2
40	ERROR-
41	A3
42	INTREQ0-
43	A4
44	INTREQ1-
45	A5
46	STROBE-
47	A6
48	ACK-
49	reserved
50	GND

IP Interface Pin Configuration

PIN	Z	A	B	C	D	E	F
1	GND	5V	-12V	TRST#	+12V	5V	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
4	GND	*BRSVP1A4*	GND	V(I/O)	INTP	INTS	GND
5	GND	*BRSVP1A5*	*BRSVP1B5*	RST#	GND	GNT#	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
12 13 14	Key Area						
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	*ACK64#*	GND
25	GND	5V	*REQ64#*	*ENUM#*	3.3V	5V	GND

PXI/CPCI J1 Pin Configuration

PIN	Z	A	B	C	D	E	F
1	GND	***PXI_LBL9***	GND	***PXI_LBL10***	***PXI_LBL11***	***PXI_LBL12***	GND
2	GND	***PXI_LBR11***	***PXI_LBR12***	SYSEN#	***PXI_LBL7***	***PXI_LBL8***	GND
3	GND	***PXI_LBR7***	GND	***PXI_LBR8***	***PXI_LBR9***	***PXI_LBR10***	GND
4	GND	V(I/O)	***PXI_RSVB4***	*C/BE[7]#*	GND	*C/BE[6]#*	GND
5	GND	*C/BE[5]#*	GND	V(I/O)	*C/BE[4]#*	*PAR64*	GND
6	GND	*AD[63]*	*AD[62]*	*AD[61]*	GND	*AD[60]*	GND
7	GND	*AD[59]*	GND	V(I/O)	*AD[58]*	*AD[57]*	GND
8	GND	*AD[56]*	*AD[55]*	*AD[54]*	GND	*AD[53]*	GND
9	GND	*AD[52]*	GND	V(I/O)	*AD[51]*	*AD[50]*	GND
10	GND	*AD[49]*	*AD[48]*	*AD[47]*	GND	*AD[46]*	GND
11	GND	*AD[45]*	GND	V(I/O)	*AD[44]*	*AD[43]*	GND
12	GND	*AD[42]*	*AD[41]*	*AD[40]*	GND	*AD[39]*	GND
13	GND	*AD[38]*	GND	V(I/O)	*AD[37]*	*AD[36]*	GND
14	GND	*AD[35]*	*AD[34]*	*AD[33]*	GND	*AD[32]*	GND
15	GND	***PXI_BRSVA15***	GND	FAL#	***PXI_LBL6***	***PXI_LBR6***	GND
16	GND	**PXI_TRIG1**	**PXI_TRIG0**	DEG#	GND	**PXI_TRIG7**	GND
17	GND	**PXI_TRIG2**	GND	PRST#	**PXI_STAR**	**PXI_CLK10**	GND
18	GND	**PXI_TRIG3**	**PXI_TRIG4**	**PXI_TRIG5**	GND	**PXI_TRIG6**	GND
19	GND	***PXI_LBL2***	GND	***PXI_LBL3***	***PXI_LBL4***	***PXI_LBL5***	GND
20	GND	***PXI_LBR4***	***PXI_LBR5***	***PXI_LBL0***	GND	***PXI_LBL1***	GND
21	GND	***PXI_LBR0***	GND	***PXI_LBR1***	***PXI_LBR2***	***PXI_LBR3***	GND
22	GND	***PXI_RSVA22***	***PXI_RSVB22***	***PXI_RSVC22***	***PXI_RSVD22***	***PXI_RSVE22***	GND

PXI/CPCI J2 Pin Configuration

NOTES: Bold-faced words are PXI defined signals.
Italicized words are unused signals.
Underlined words are used by the system slot.

APPENDIX B - PCI CONFIGURATION REGISTERS

The configuration registers contain basic information needed to configure a PXI/CPCI system. **This information is provided for reference only.** For complete information, please refer to the latest PCI Specification.

IP Configuration Registers

A16 Address	Register Description
Base + 00	Vendor ID*
Base + 02	Device ID*
Base + 04	Command*
Base + 06	Status*
Base + 08	Revision ID
Base + 09	Class Code
Base + 0C	Cache Line Size
Base + 0D	Latency Timer
Base + 0E	Header Type
Base + 0F	BIST
Base + 10	Base Address Registers*
Base + 28	Cardbus CIS Pointer
Base + 2C	Subsystem Vendor ID
Base + 2E	Subsystem ID
Base + 30	Expansion ROM Based Address
Base + 34	CAP_PTR
Base + 35	Reserved
Base + 3C	Interrupt Line*
Base + 3D	Interrupt Pin*
Base + 3E	Min_Gnt
Base + 3F	Max_Lat

* Bit details provided below.

Vendor (ID) Register (Base + 00_{16}) This read-only register provides vendor identification and is assigned by the PCI Special Interest Group.

Device (ID) Register (Base + 02_{16}) This read-only register provides the vendor identifier. The vendor ID is assigned by the vendor.

Command Register (Base + 04_{16}) This read/write register is used to control the devices ability to respond to bus accesses.

Status Register (Base + 06_{16}) This read-only register is used by the device to record any catastrophic event that might interrupt normal operation.

Revision (ID) Register (Base + 08_{16}) This read-only register is supplied by the vendor in order to indicate the revision level of the device.

Class Code Register (Base + 09_{16}) This read-only register provides information concerning the generic function of the device.

Cache Line Size Register (Base + $0C_{16}$) This read-only register provides information on the cacheline length. This register is used during bursting. This register is not used in this application and should be ignored.

Latency Timer Register (Base + $0D_{16}$) This read/write register is used to define the maximum amount of time that a device can control the bus in times of heavy traffic.

Header Type Register (Base + $0E_{16}$) This read-only register provides information concerning the header type of the device. This also specifies whether the device is multifunctional or not. For our application the header type that we will use is 00H.

PXI BIST Register (Base + $0F_{16}$) This read/write register invokes and reports the results of the built in self-test. If the device does not support this function, then a 00H must be returned.

Base Address Registers (Base + 10_{16}) This read/write register is used to dynamically configure memory for a specific device. The header space reserves 24 bytes dedicated for defining memory and I/O space.

Cardbus CIS Pointer Register (Base + 28_{16}) This read-only register is used for devices that share silicon between cardbus and PCI. Cardbus cards use Card Information Structure that provides information about the card. This register is optional and is not used in this device.

Subsystem Vendor (ID) Register (Base + $2C_{16}$) This read-only register allows the vendor to uniquely identify any subsystem that may share the same PCI controller. This register is optional

Subsystem (ID) (Base + $2E_{16}$) This read-only register provides the vendor to uniquely classify and identify a subsystem that shares the same PCI Controller. This register is optional.

Expansion ROM Based Address Register (Base + 30_{16}) This read/write register is used to allocate expansion ROM and for our purposes will not be necessary and should be disabled by writing a ‘0’ to bit (0) of the register.

CAP PTR Register (Base + 34_{16}) This read-only register is used to point to a list of data structures that define the PCI functions new capabilities such and AGP and PCI power management. This register is qualified by Bit (4) of Register (06H). This device does not support this register.

Reserved Register (Base + 35_{16}) This register is reserved.

Interrupt Line Register (Base + $3C_{16}$) This read/write register identifies which line of a system interrupt controller the devices interrupt line is connected to. This is described below.

Interrupt Pin Register (Base + $3D_{16}$) This read-only register identifies which interrupt pin the device is using.

Min Gnt Register (Base + $3E_{16}$) This read-only register specifies the burst period required by the device. This value is used to determine latency timer values.

Max Lat Register (Base + $3F_{16}$) This read-only register specifies how often the device needs to gain access to the PCI bus. This value is used to determine latency timer values.

Vendor ID

00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Only	Vendor Number															

Manuf. ID ⇨ Manufacturer Identification (C&H = $162C_{16}$)

Device ID

02

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Only	Device Number															

Device Number ⇨ Device Number (PX403S = $403A_{16}$)

Command

04

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Reserved						R/W	SER	STP	PAR	PAL	BWR	SPC	BUS	MEM	I/O
Read							R/W	SER	STP	PAR	PAL	BWR	SPC	BUS	MEM	I/O

R/W ⇨ Read/Write for Back to Back Transactions (1 = Enables transactions)
SER ⇨ SERR Driver Control (1 = Enables system error output driver)
STP ⇨ Address Data Stepping (1 = Enables address Stepping)
PAR ⇨ Parity Control (1 = Responds to parity errors)
PAL ⇨ Palate Snooping (This bit is not implemented)
BWR ⇨ Bus Master Validation (1 = Bus masters generate write and invalidate command, 0 = Memory write is used instead)
SPC ⇨ Special Cycle Control (1 = Monitors special cycle operations)
BUS ⇨ Bus Master Control (1 = Enable device to generate bus accesses) Used by bus master.
MEM ⇨ Memory Access (1 = Enable memory space accesses)
I/O ⇨ I/O Space Access (1 = Enables I/O space accesses)

Status

06

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	DPE	SSE	RMA	RTA	STA	——		DPS	—	—	—	—	Reserved			
Read	DPE	SSE	RMA	RTA	STA	DST		DPS	FBB	UDF	66S	NCS				

DPE ⇨ Detected Parity Error (1 = Parity error detected)
SSE ⇨ Signaled System Error Status (1 = System error detected)
RMA ⇨ Received Master Abort Status (1 = Bus master abort terminated a bus master transaction)
RTA ⇨ Received Target Abort Status (1 = Target abort terminated bus master transaction)
STA ⇨ Signaled Target Abort Status (1 = Target device terminated transaction with target abort)
DST ⇨ Device Select Timing Status
00H = Asserts DEVSEL in fast timing Mode
01H = Asserts error has DEVSEL in medium timing Mode
10H = Asserts DEVSEL in slow timing Mode
11H = Reserved
DPS ⇨ Data Parity Status (1 = parity occurred)
FBB ⇨ Fast Back-to-Back Status (1 = capable of fast-back-to-back transactions)
UDF ⇨ User Definable Features Status (1 = supported)
66S ⇨ 66MHz Capable status (0 = device is running at 33MHz, 1 = device is running at 66MHz)
NCS ⇨ New Capabilities (1 = supports New Capabilities)

Note: This register is only write capable for clearing and not setting bits.

Base Address Register

10

Bit	31	4	3	2	1	0
Write	Memory Base Address		—	———		—
Read	Memory Base Address		PRF	MEMTYPE		ASI

Memory Base Address ⇨ Memory Base Address (Upper 28 bits base address)
MEMTYPE ⇨ Memory Type (This device uses memory type 00_{16})
PRF ⇨ Perfectible (0 = Memory is not perfectible)
ASI ⇨ Address Space Indicator (0 = Memory Space, 1 = I/O Space)

Note: PXI Base Address Register is a 32 Bit register.

Interrupt Line / Interrupt Pin

3C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	(Read only)								Interrupt Line							
Read	Interrupt Pin								Interrupt Line							

Interrupt Pin ⇨ Interrupt pin to use

00_{16}	Not used
01_{16}	INTA#
02_{16}	INTB#
03_{16}	INTC#
04_{16}	INTD#
05_{16}:FE_{16}	Reserved

Interrupt Line ⇨ Interrupt line the device is connected to. (00_{16}:FE_{16}, FF_{16} = Device is not connected to a system)

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