PX451S PXI Digital Input Event Detector

Assembly P/N 11029180

DESCRIPTION

The PX451S is a 16 or 32 channel digital input module that samples and selectively stores up to 32 bits of digital data along with a 31-bit time stamp at a rate up to 5 MHz. The 31-bit time tag allows unique time tagged data. The module has the ability to store all data at the specified sample rate or selectively store input values based upon changes in state of one or more of the inputs.

The PX451S is an integration of one or two MA203 modules and an AMi3002 PXI M-module carrier. One MA203 is used for the -0001 16-channel version and two MA203's are used for the -0002 32-channel version. Each MA203 provides 16 channels of programmable threshold event detection. The carrier provides the electrical and mechanical interface to a PXI backplane and chassis.



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SOFTWARE CONFIGURATION AND CONTROL

A software driver for the PX451S is available for download on C&H's website. The driver uses the VISA I/O library and includes an interactive soft front panel that can be used to operate the PX451S. The driver provides a library of function calls for initializing, configuring, and operating the instrument. The library is provided in formats for most popular development environments as well as in a Windows DLL format.

Also available for download on C&H's website is the Interactive Mezzanine Control (IMC) software. IMC is a Windows application that provides low-level access to any mezzanine module on any one of C&H's carriers. IMC can be a very useful tool during software development and debug.

SPECIFICATIONS

Number of Chann	els: 16 or 32
Sample Rate:	up to 5MHz
Input Debounce:	0 to 128ms Software selectable

Input Specifications:

Threshold Resolution	100mV
Threshold Range	0 – 25.6V
Threshold Accuracy	±0.5% of FS
Max. Input Voltage	28V
Input Hysteresis	25mV

Input Masking:

Any bit is pattern programmable

Local Memory:

32K x 48 (31-bit timestamp)

Sampling Strobe:

- Internal: To 5 MHz
- Front Panel: To 5 MHz
- Backplane Trigger: To 5 MHz
- (Source & prescaler software programmable)

Interrupts:

- Data Stored
- FIFO Half-Full
- FIFO Full
- Time-Stamp Rollover
- Preset Change of State
- Preset Level Transition
- Preset Bit Pattern

I/O Connector:

• 44-pin DSUB (female)

ELECTRICAL

The electrical interface is compliant with the PXI bus specification Rev 2.1, cPCI Specification 2.0 R3.0, and PCI Specification 2.2 (slave only). The module supports both 5V and 3.3V signaling voltages (VIO). Five PXI compliant trigger lines are supported.

Power Requirements: (-0001/-0002)

+5V	800mA / 1.2A
+12V	0mA / 0mA
-12V	20mA / 40mA

MECHANICAL

To allow the use of two M-modules in a standard 3U cPCI (PXI) system, the module is slightly higher than the 3U standard. The card guide rails for the slot the module will be used in must be replaced with the special card guide rails supplied with the PX451S. The rails easily snap out using a flat screwdriver.

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ENVIRONMENTAL

Operating Temperature:	0°C to +50°C
Storage Temperature:	-40°C to +70°C
Humidity:	<95% without condensation

DOCUMENTATION

This document discusses the general use of the PX451S integrated module. For full details on each of the individual modules used in the PX451S, please refer to the User Manual for that particular module.

Document Description	Website
MA203 User Manual	www.chtech.com -> Support -> Product Manuals -> Measurement -> MA203
i3002 User Manual	www.acq.nl -> Products -> Carrier -> i3002-> Manual

The MA203 User Manual discusses several types of input accessory modules; however, the PX451S comes configured with the programmable threshold module (Opt. 4) only. Use Appendix E – AM104 Opt. 4 for the signal conditioning specifications and operation.

HARDWARE CONFIGURATION

The default MA203 Factory Switch Settings are:

External Clock Impedance:	50Ω
External Clock Threshold Level:	TTL (0.8V)
External Run Impedance:	50Ω
External Run Threshold Level:	TTL (0.8V)

SYNCHRONIZATION

The MA203 has several features that support synchronization of the channels when using the full 32 channel (-0002) version of the PX451S.

- a) If external clocking is used, then synchronization can be done by simply connecting the external signal to both the EXTCLK0 and EXTCLK1. To ensure proper impedance control, the input impedance of one MA203 should be switched to >100K Ω (high) and the other left on 50 Ω .
- b) If backplane trigger clocking is used, simply set both MA203's to trigger on the same backplane trigger (A or B) and on the same edge.
- c) If internal clocking is used, one MA203 is used as the master clock with its clock output to a trigger signal. Both MA203's are then configured to use the same trigger for its sample clock.

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I/O CONNECTOR

Below is the signal list for the two connectors located on the front panel of the PX451S. For more details on each signal, please refer to the MA203 User Manual.

	16	\nearrow		т					
1	17	31		Top Connector (-0002 only)					
2	18	32	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	
3		33	1	INA16(+)	16	GND	31	GND	
4	19	34	2	INA17(+)	17	GND	32	-12VSUP1*	
-	20	05	3	INA18(+)	18	GND	33	+12VSUP1*	
5	21	35	4	INA19(+)	19	GND	34	GND	
6	22	36	5	INA20(+)	20	GND	35	ISOVNEG1*	
7		37	6	INA21(+)	21	GND	36	ISOVPOS1*	
8	23	38	7	INA22(+)	22	GND	37	GND	
	24		8	INA23(+)	23	GND	38	EXTCLK1	
9	25	39	9	INA24(+)	24	GND	39	GND	
10	26	40	10	INA25(+)	25	GND	40	EXTRUN1	
11	20	41	11	INA26(+)	26	GND	41	GND	
12	27	42	12	INA27(+)	27	GND	42	GND	
10	28		13	INA28(+)	28	GND	43	GND	
13	29	43	14	INA29(+)	29	GND	44	INA31(+)	
14	30	44	15	INA30(+)	30	GND			
15	50		1						



	16	\searrow			Datta		4	
1	17	31		Bottom Connector				
2	18	32	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
3	40	33	1	INA0(+)	16	GND	31	GND
4	19	34	2	INA1(+)	17	GND	32	-12VSUP0*
-	20		3	INA2(+)	18	GND	33	+12VSUP0*
5	21	35	4	INA3(+)	19	GND	34	GND
6	22	36	5	INA4(+)	20	GND	35	ISOVNEG0*
7	22	37	6	INA5(+)	21	GND	36	ISOVPOS0*
8	23	38	7	INA6(+)	22	GND	37	GND
Ũ	24	50	8	INA7(+)	23	GND	38	EXTCLK0
9	25	39	9	INA8(+)	24	GND	39	GND
10	20	40	10	INA9(+)	25	GND	40	EXTRUN0
11	26	41	11	INA10(+)	26	GND	41	GND
12	27	40	12	INA11(+)	27	GND	42	GND
12	28	42	13	INA12(+)	28	GND	43	GND
13	29	43	14	INA13(+)	29	GND	44	INA15(+)
14	20	44	15	INA14(+)	30	GND		()
15	30		* These	e output pins are o	only used for	r supplemental	operation.	

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